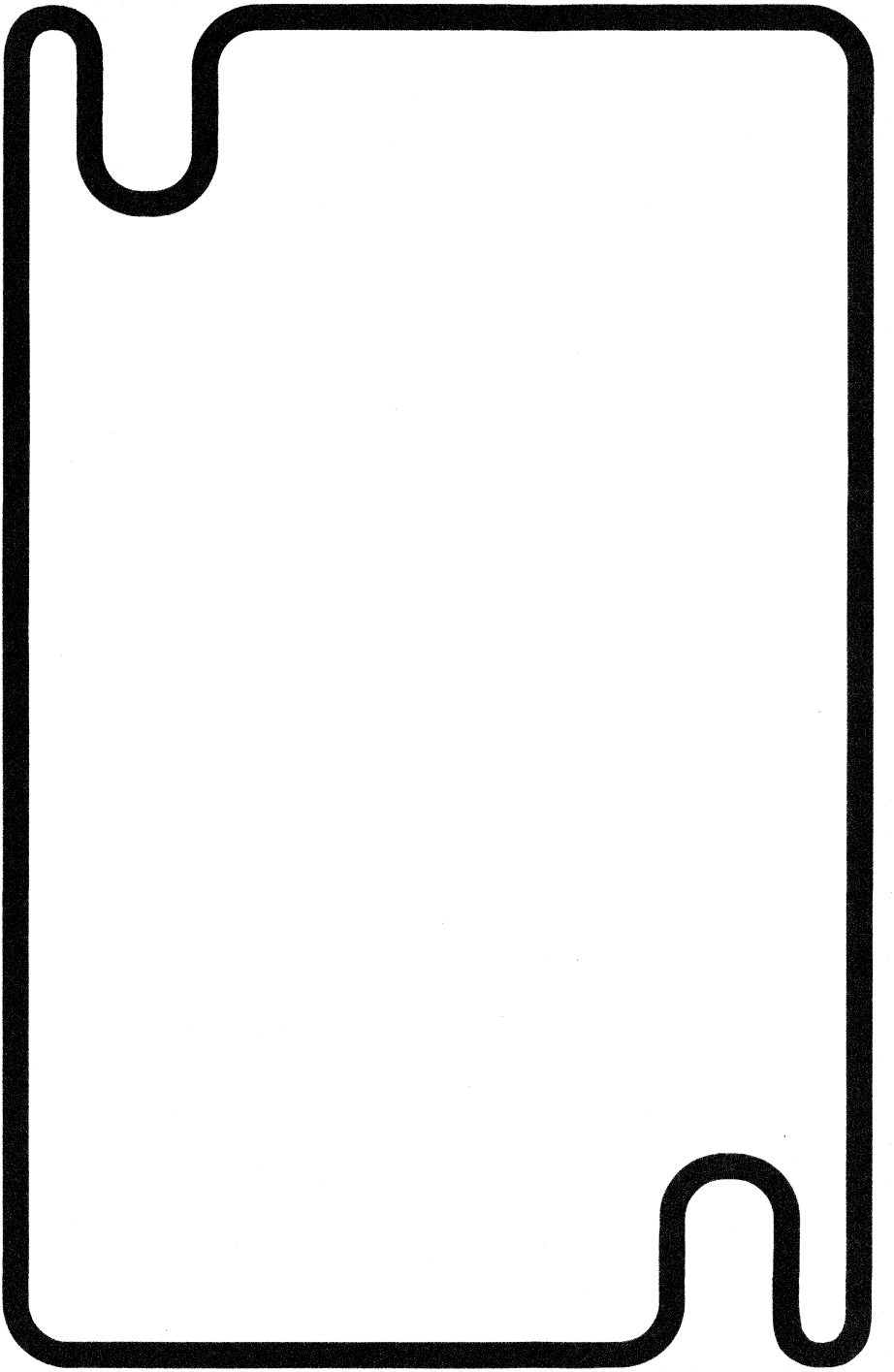


CONTENTS

BIPOLAR CONTENTS—

TTL PROM

Commercial (0°C to + 75°C)

Type No.		Function		Max. Access	Page
N82S23	32 x 8	Open Collector	PROM	50ns	5
N82S123	32 x 8	Tri-state	PROM	50ns	5
N82S126	256 x 4	Open Collector	PROM	50ns	9
N82S129	256 x 4	Tri-state	PROM	50ns	9
N82S27	256 x 4	Open Collector	PROM	40ns	13
N82S130	512 x 4	Open Collector	PROM	50ns	17
N82S131	512 x 4	Tri-state	PROM	50ns	17
N82S114	256 x 8	Tri-state	PROM	60ns	21
N82S115	512 x 8	Tri-state	PROM	60ns	21

Military (−55°C to + 125°C)

Type No.		Function		Max. Access	Page
S82S23	32 x 8	Open Collector	PROM	65ns	5
S82S123	32 x 8	Tri-state	PROM	65ns	5
S82S126	256 x 4	Open Collector	PROM	70ns	9
S82S129	256 x 4	Tri-state	PROM	70ns	9
S82S130	512 x 4	Open Collector	PROM	80ns	17
S82S131	512 x 4	Tri-state	PROM	80ns	17
S82S114	256 x 8	Tri-state	PROM	To be announced	
S82S115	512 x 8	Tri-state	PROM		

TTL Field Programmable Logic Array

Commercial (0°C to + 75°C)

Type No.		Function		Page
N82S100	16 x 48 x 8	Tri-state	FPLA	26
N82S101	16 x 48 x 8	Open Collector	FPLA	26

ECL PROM

Extended Commercial (−30°C to +85°C)

Type No.		Function	Max. Access	Page
10139	32 x 8	PROM	20ns	31
10149	256 x 4	PROM	To be announced	

TTL ROM

Commercial (0°C to +70°C)

Type No.		Function	Max. Access	Page
N82S226	256 x 4	Open Collector ROM	50ns	37
N82S229	256 x 4	Tri-state ROM	50ns	37
N82S230	512 x 4	Open Collector ROM	50ns	40
N82S231	512 x 4	Tri-state ROM	50ns	40
N82S214/ 8204	256 x 8	Tri-state ROM	75ns	43
N82S215/ 8205	512 x 8	Tri-state ROM	75ns	43
N8228	1024 x 4	ROM	70ns	46

Military (−55°C to +125°C)

Type No.		Function	Max. Access	Page
S82S226	256 x 4	Open Collector ROM	70ns	37
S82S229	256 x 4	Tri-state ROM	70ns	37
S82S230	512 x 4	Open Collector ROM	80ns	40
S82S231	512 x 4	Tri-state ROM	80ns	40
S82S214	256 x 8	Tri-state ROM	To be announced	
S82S215	512 x 8	Tri-state ROM		

MOS CONTENTS –

signetics

256-BIT BIPOLAR PROGRAMMABLE ROM (32x8 ROM) (82S23 OPEN COLLECTOR) (82S123 TRI-STATE)

82S23
82S123

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

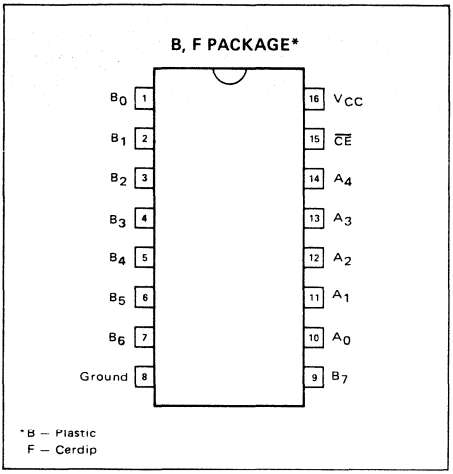
DESCRIPTION

The 82S23 (Open Collector Outputs) and the 82S123 (Tri-State Outputs) are Bipolar 256-Bit Read Only Memories, organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S23 and 82S123 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, B or F. For the military temperature range (−55°C to +125°C) specify S82S23/123, F only.

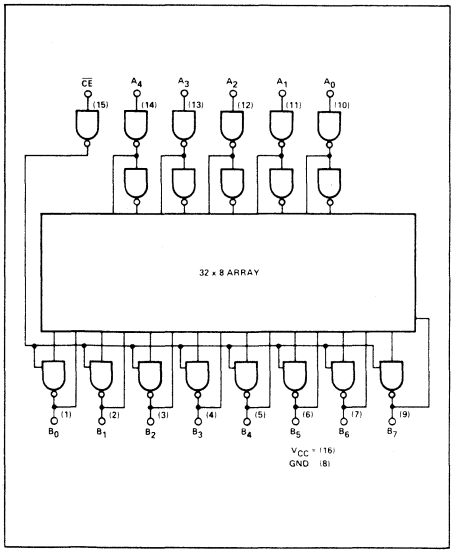
PIN CONFIGURATION



FEATURES

- ORGANIZATION – 32 X 8
- ADDRESS ACCESS TIME:
  - S82S23/S82S123 – 65ns, MAXIMUM
  - N82S23/N82S123 – 50ns, MAXIMUM
- POWER DISSIPATION – 1.3mW/BIT TYPICAL
- INPUT LOADING:
  - S82S23/123 – (−150μA) MAXIMUM
  - N82S23/123 – (−100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - OPEN COLLECTOR – 82S23
  - TRI-STATE – 82S123
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

LOGIC DIAGRAM



APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
FORMAT CONVERSION
HARDWIRED ALGORITHMS
RANDOM LOGIC
CODE CONVERSION

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S23)	+5.5	Vdc
V_O	Off-State Output Voltage (82S123)	+5.5	Vdc
T_A	Operating Temperature Range (N82S23/123) (S82S23/123)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S23/S82S123 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S23/N82S123 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S23/S82S123			N82S23/N82S123			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.45	V
I_{OLK}	Output Leakage Current (82S23)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			50			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S123)	$\overline{CE}$ = "1", V_{OUT} = 5.5V $\overline{CE}$ = "1", V_{OUT} = 0.5V			50 −50			40 −40	μA μA
V_{OH}	"1" Output Voltage (82S123)	$\overline{CE}$ = "0", I_{OUT} = −2mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			50	μA
V_{IL}	"0" Level Input Voltage				0.8			0.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			65	85		65	77	mA
V_{IC}	Input Clamp Voltage	I_N = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S123)	V_{OUT} = 0V	−20		−100	−20		−90	mA

SWITCHING CHARACTERISTICS

S82S23/S82S123 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S23/N82S123 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S23/S82S123			N82S23/N82S123			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		35	65		35	50	ns
T_{CD}	Chip Disable to Output			25	40		25	35	ns
T_{CE}	Chip Enable to Output			25	40		25	35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

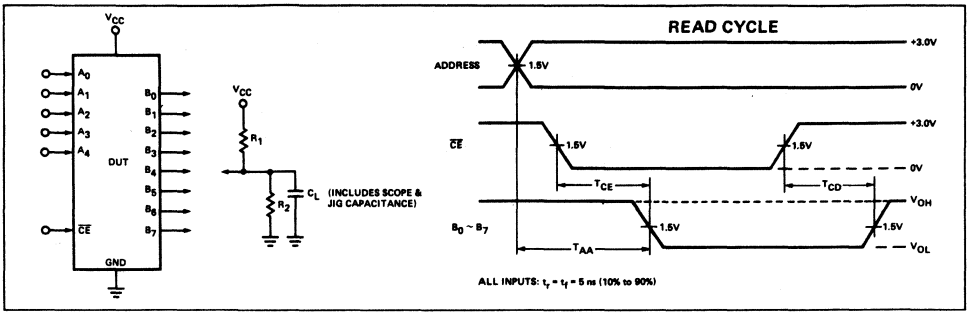
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 250 ± 50mA (Transient or steady state)	9.5	10.0	10.5	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +10.0 ± 0.5V	200	250	300	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	μA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	μA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 65 ± 3mA (Transient or steady state)	15.0	15.5	16.0	V
I_{OUT}	Output Programming Current	V_{OUT} = +15.5 ± 0.5V	62	65	68	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_V	Verify Delay		50			μs
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

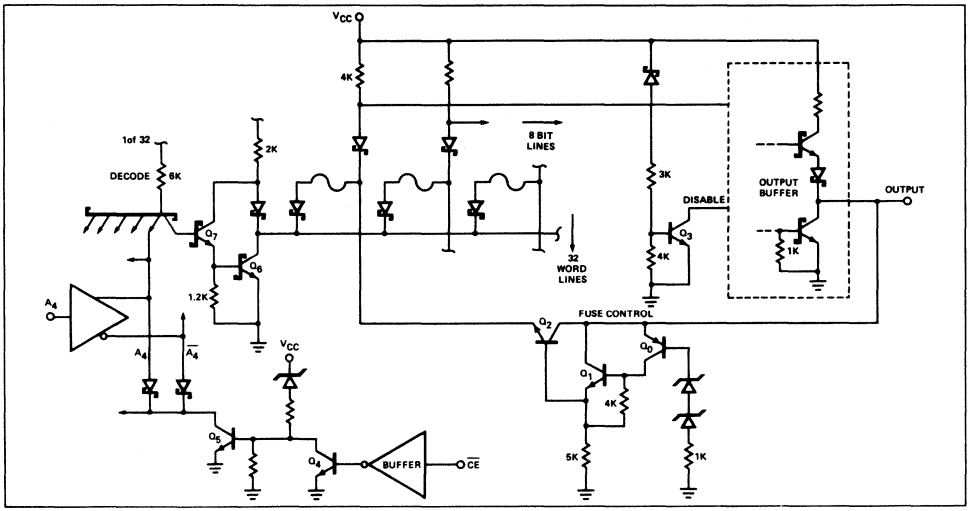
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = +10 ± 0.5V.
3. After 10μs delay, apply I_{OUT} = 65 ± 3mA to the output to be programmed. Program one output at a time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove I_{OUT} from the programmed output.
6. After 10μs delay, return V_{CC} to 0V.
7. To verify programming, after 50μs delay, raise V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
8. Raise V_{CC} to V_{CCP} = +10 ± 0.5V and repeat steps 3 through 7 to program other bits at the same address.
9. After 10μs delay, repeat steps 2 through 8 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure that +15.5 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.

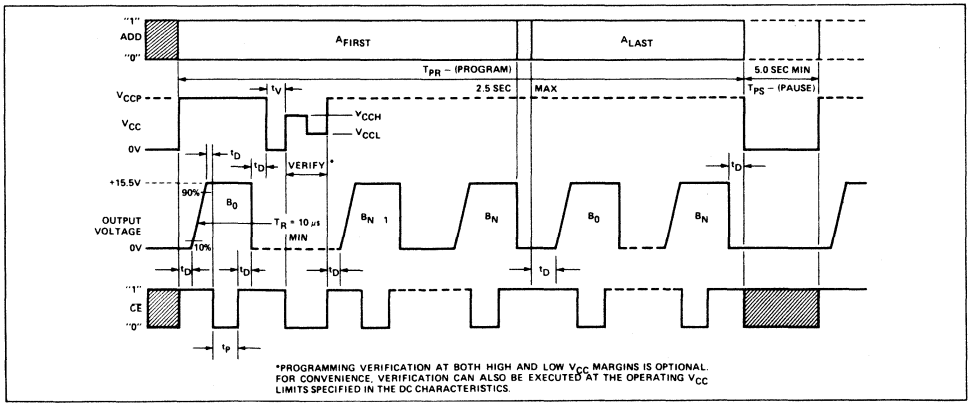
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

signetics

1024-BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

82S126
82S129

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S126 (Open Collector Outputs) and the 82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S126 and 82S129 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, B or F. For the military temperature range (−55°C to +125°C) specify S82S126/129, F only.

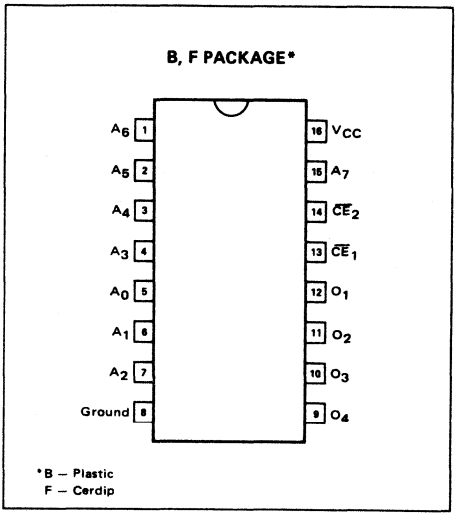
FEATURES

- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME:
  - S82S126/129 – 70ns, MAXIMUM
  - N82S126/129 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT TYPICAL
- INPUT LOADING:
  - S82S126/129 – (−150μA) MAXIMUM
  - N82S126/129 – (−100μA) MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  - OPEN COLLECTOR – 82S126
  - TRI-STATE – 82S129
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

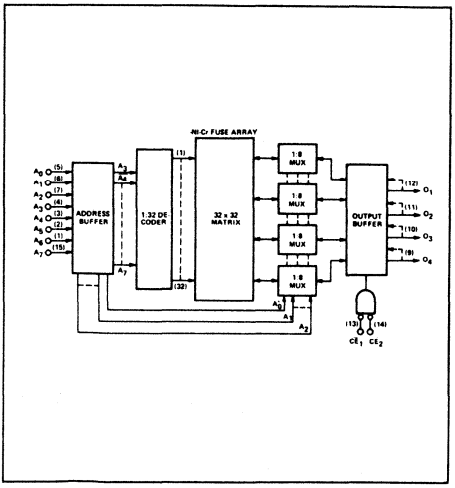
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S126)	+5.5	Vdc
V_O	Off-State Output Voltage (82S129)	+5.5	Vdc
T_A	Operating Temperature Range (N82S126/129) (S82S126/129)	 0° to +75° -55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S126/S82S129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/N82S129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.5	V
I_{OLK}	Output Leakage Current (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 0.5V			-60			-40	μA
V_{OH}	"1" Output Voltage (82S129)	$\overline{CE}_1$ = $\overline{CE}_2$ = "0", I_{OUT} = -2.0mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			-150			-100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			105	125		105	120	mA
V_{IC}	Input Clamp Voltage	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
I_{OS}	Output Short Circuit Current (82S129)	V_{OUT} = 0V	-15		-85	-20		-70	mA

SWITCHING CHARACTERISTICS

S82S126/129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		35	70		35	50	ns
T_{CD}	Chip Disable to Output			15	35		15	20	ns
T_{CE}	Chip Enable to Output			15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

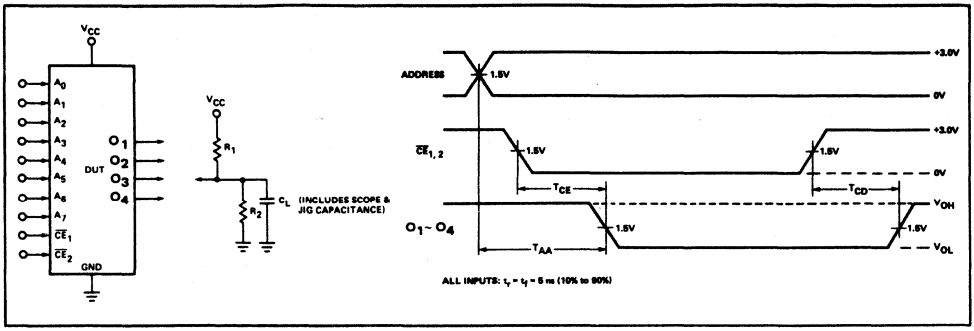
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 350 ± 50mA (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +8.75 ± .25V	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	μA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	μA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 200 ± 20mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	V_{CC} = V_{CCP}			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

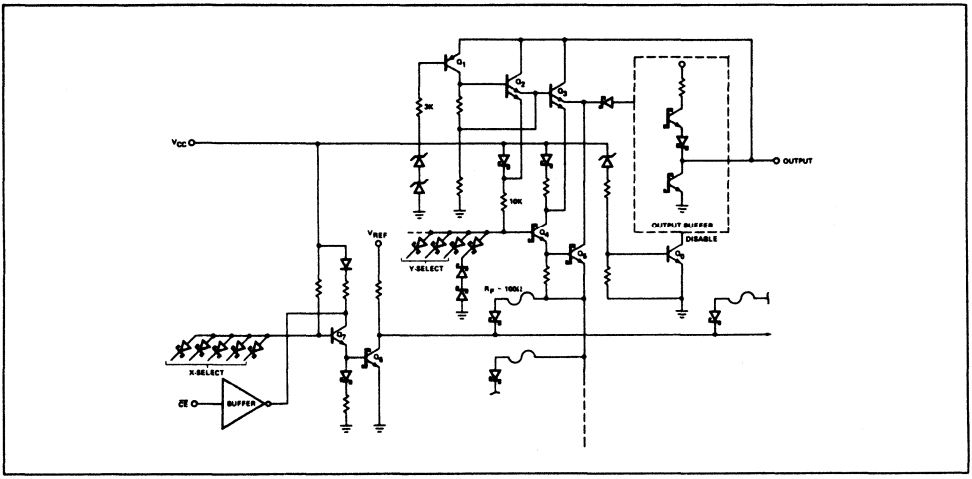
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.

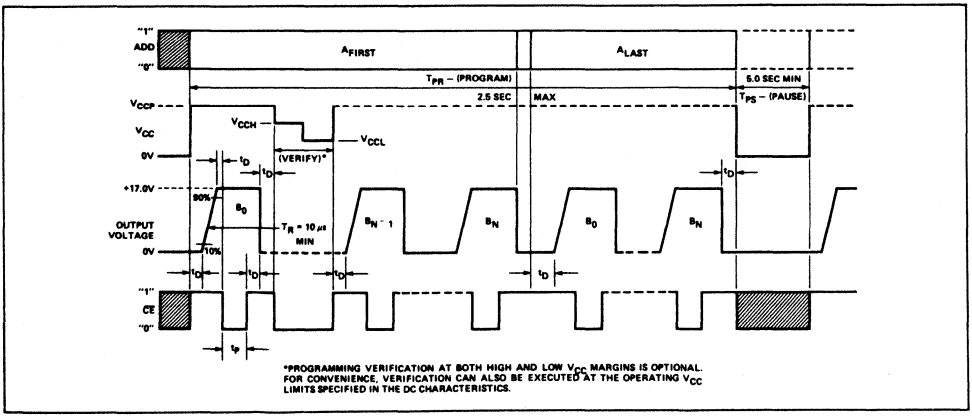
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

signetics

1024-BIT BIPOLAR PROGRAMMABLE ROM (256X4 PROM) | 82S27

JULY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

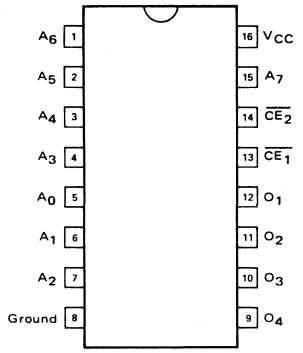
The 82S27 is a Bipolar 1024-Bit Read Only Memory, organized as 256 words by 4 bits per word. It is Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S27 is supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S27 is fully TTL compatible, and includes on-chip decoding, two chip enable inputs, and open collector outputs for ease of memory expansion.

The 82S27 is available in the commercial temperature range. For the commercial temperature range (0°C to +75°C) specify N82S27, F.

PIN CONFIGURATION

F PACKAGE*

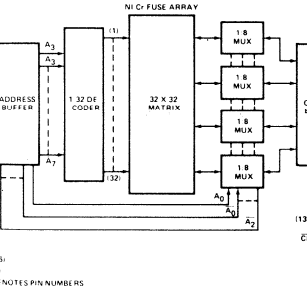


*F = Cerdip

FEATURES

- ORGANIZATION – 256 X 4
- ADDRESS ACCESS TIME – 40ns, MAXIMUM
- POWER DISSIPATION – 0.6mW/BIT, TYPICAL
- INPUT LOADING – 1.6mA, MAXIMUM
- TWO CHIP ENABLE INPUTS
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

BLOCK DIAGRAM



APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 32mA		0.45	0.50	V
I_{OLK}	Output Leakage Current	$\overline{CE_1}$ or $\overline{CE_2}$ = "1", V_{OUT} = 5.5V			100	μA
I_{IH}	"1" Input Current	V_{IN} = 2.4V			40	μA
		V_{IN} = 5.5V			1	mA
I_{IL}	"0" Input Current	V_{IN} = 0.50V			−1.6	mA
V_{IL}	"0" Level Input Voltage				.80	V
V_{IH}	"1" Level Input Voltage		2.0			V
I_{CC}	V_{CC} Supply Current			120	140	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −12mA		−1.0	−1.5	V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V, $\overline{CE_1}$ or $\overline{CE_2}$ = "1"		8		pF

SWITCHING CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{AA}	Address to Output	C_L = 30pF		30	40	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^{\circ}C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 300 ± 50mA (Transient or steady state)	5.0		5.25	V
V_{CCH}	Upper Verify Limit		5.0	5.25	5.5	V
V_{CCL}	Lower Verify Limit		4.5	4.75	5.0	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +5.0 ± 0.25V	250	300	350	mA
Input Voltage						
V_{IH}	Logical "1" (Except $\overline{CE_1}$)		3.0		5.0	V
V_{IN}	Program Level ($\overline{CE_1}$ Only)		14.0	14.5	15.0	V
V_{IL}	Logical "0"		0	0.4	0.5	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +3.0V			100	μA
I_{IL}	Logical "0"	V_{IL} = +0.5V			-1.6	mA
I_{IN}	Program Level ($\overline{CE_1}$ Only)	V_{IN} = +15.0V			15	mA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 115 ± 10mA (Transient or steady state)	16.5	17.0	17.5	V
I_{OUT}	Output Programming Current	V_{OUT} = +17.0 ± 0.5V	105	115	125	mA
T_R[5]	Output Pulse Rise Time		0.2		0.5	μs
t_P	Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10kΩ resistor to V_{CC}.

c. Set $\overline{CE_2}$ to logic "0".

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to $\overline{CE_1}$ (pin 13) a voltage source of 14.5 ± 0.5V, with 15mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 0.5V to the output to be programmed. The source must have a current limit of 115mA. Program one output at the time.

Step 4 After 10μs delay, remove +17.0V supply from programmed output.

Step 5 To verify programming, after 10μs delay, return $\overline{CE_1}$ to 0V. Raise V_{CC} to V_{CCH} = +5.25 ± .25V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.75 ± .25V, and verify that the programmed output remains in the "1" state.

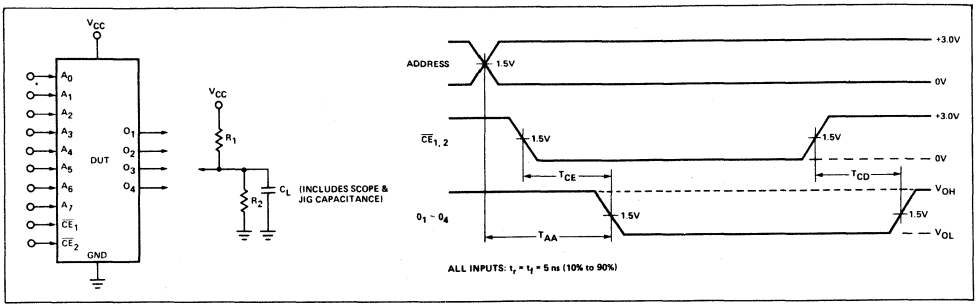
Step 6 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 5 to program other bits at the same address.

Step 7 Repeat steps 1 through 6 to program all other address locations.

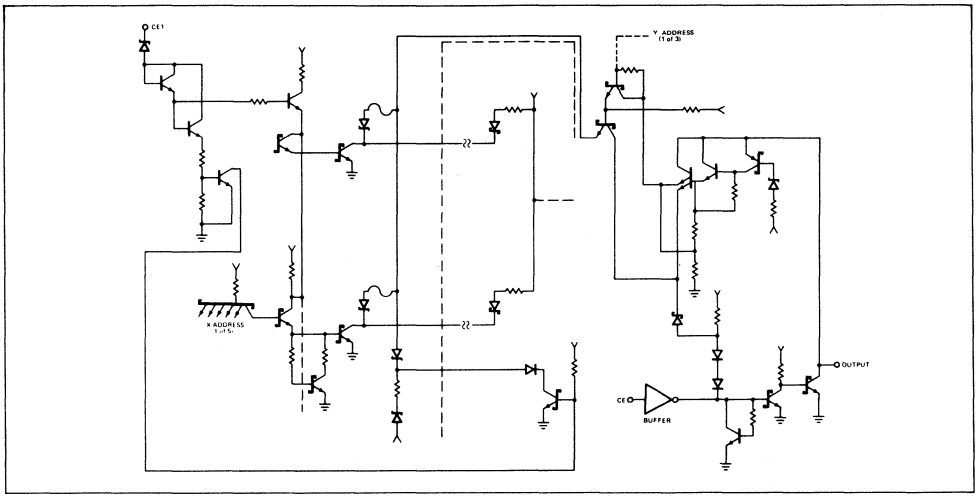
NOTES:

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.
5. Measured with a 1k dummy load connected across the fusing source.

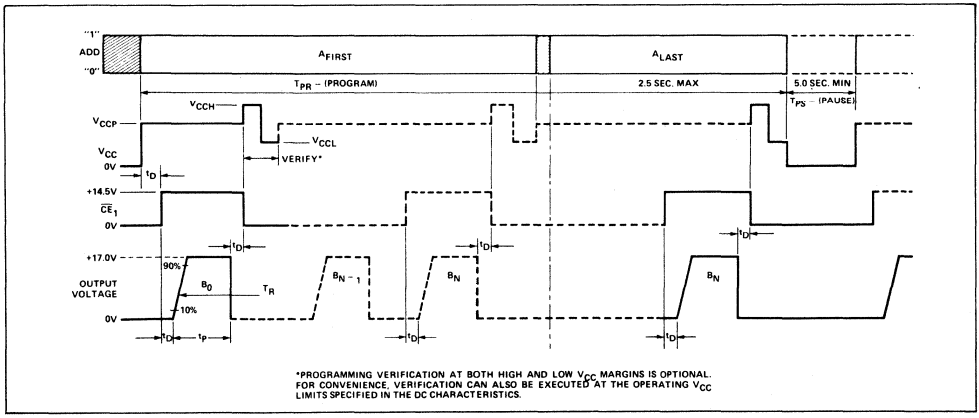
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

signetics

2048-BIT BIPOLAR PROGRAMMABLE ROM (512x4 PROM)

82S130
82S131

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S130 (Open Collector Outputs) and the 82S131 (Tri-State Outputs) are Bipolar 2048-Bit Read Only Memories, organized as 512 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S130 and 82S131 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S130/131, F. For the military temperature range (−55°C to +125°C) specify S82S130/131, F.

FEATURES

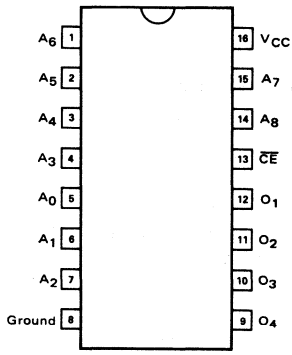
- ORGANIZATION – 512 X 4
- ADDRESS ACCESS TIME:
  - S82S130/131 – 70ns, MAXIMUM
  - N82S130/131 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.3mW/BIT TYPICAL
- INPUT LOADING:
  - S82S130/131 – (−150μA) MAXIMUM
  - N82S130/131 – (−100μA) MAXIMUM
- ONE CHIP ENABLE INPUT
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  - 82S130 – OPEN COLLECTOR
  - 82S131 – TRI-STATE
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

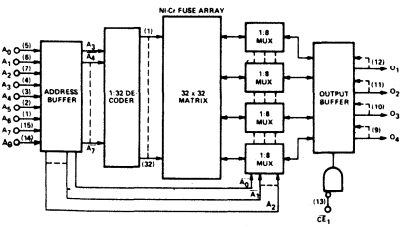
PIN CONFIGURATION

F PACKAGE*



*F – Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S130)	+5.5	Vdc
V_O	Off-State Output Voltage (82S131)	+5.5	Vdc
T_A	Operating Temperature Range (N82S130/131) (S82S130/131)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S130/131 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S130/131 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S130/131			N82S130/131			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.45	V
I_{OLK}	Output Leakage Current (82S130)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S131)	$\overline{CE}$ = "1", V_{OUT} = 0.5V $\overline{CE}$ = "1", V_{OUT} = 5.5V			−60 60			−40 40	μA μA
V_{OH}	High Level Output Voltage (82S131)	$\overline{CE}$ = "0", I_{OUT} = −2.4mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			120	140		120	140	mA
V_{IC}	Input Clamp Voltage	I_N = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S131)	V_{OUT} = 0V	−15		−85	−20		−70	mA

SWITCHING CHARACTERISTICS

S82S130/131 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S130/131 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S130/131			N82S130/131			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		35	70		35	50	ns
T_{CD}	Chip Disable to Output			20	30		20	30	ns
T_{CE}	Chip Enable to Output			20	30		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

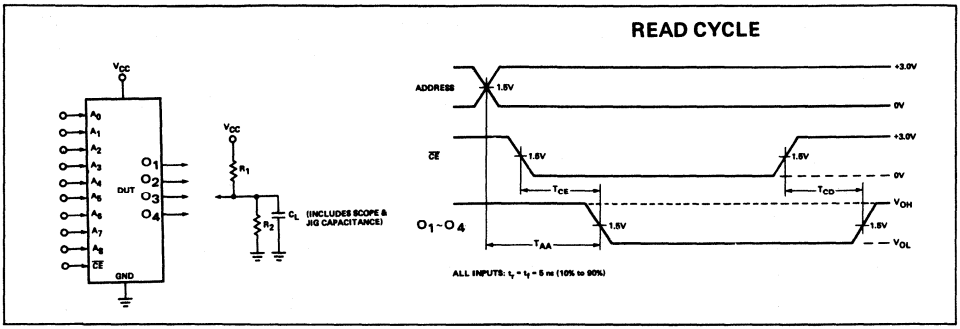
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 350 ± 50mA (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +8.75 ± .25V	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	μA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	μA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 200 ± 20mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}[5]	Programming Time	V_{CC} = V_{CCP}			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

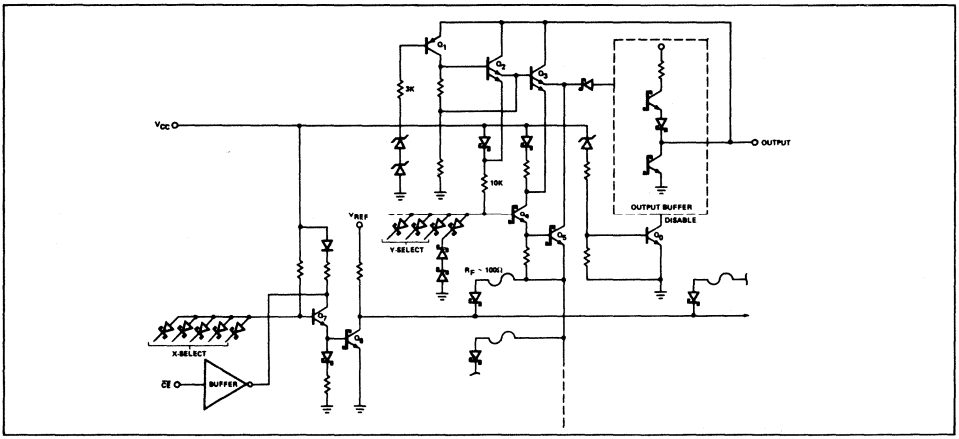
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.

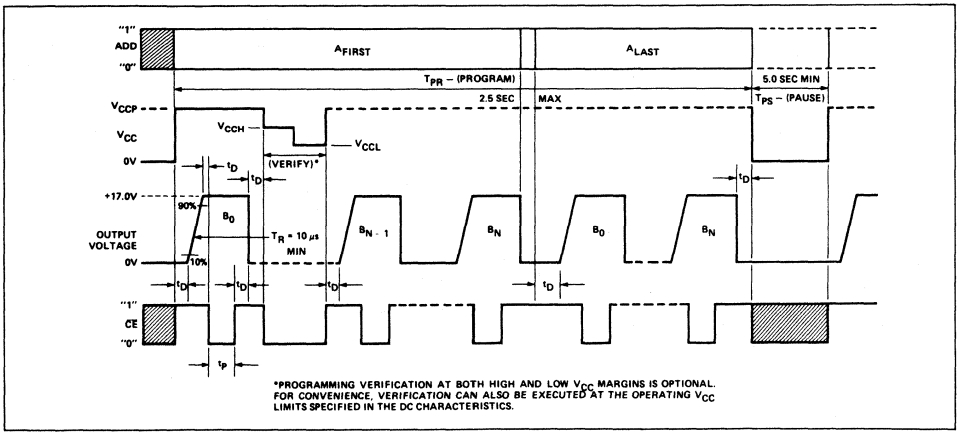
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



signetics

2048-BIT BIPOLAR ROM (256x8 PROM)
4096-BIT BIPOLAR ROM (512x8 PROM)

82S114
82S115

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S114 and 82S115 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S114 and 82S115 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S114 and 82S115 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines. In the LATCHED READ mode, after the desired address is applied and both $\overline{CE1}$ and CE2 are enabled, data will enter the output latches following the positive transition of STROBE, and the data out lines will be locked into their last valid state following the negative transition of STROBE. The latches will remain set and the outputs enabled until the chip is disabled and STROBE is brought high.

Both 82S114 and 82S115 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify. N82S114/115, I.

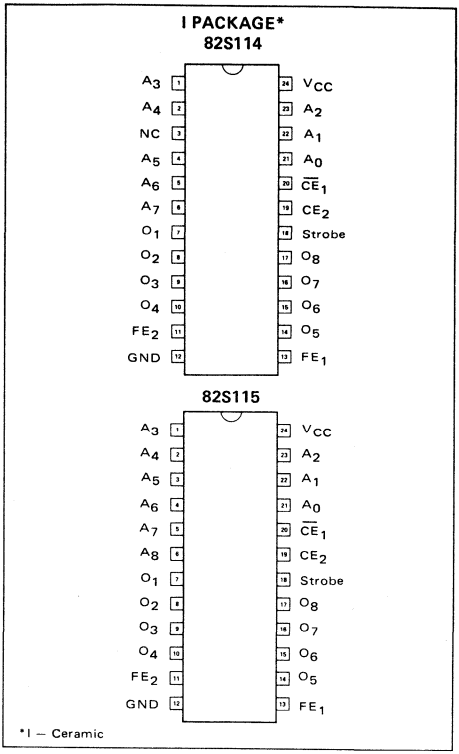
FEATURES

- ORGANIZATION:
  - 82S114 – 256 X 8
  - 82S115 – 512 X 8
- ADDRESS ACCESS TIME – 60ns, MAXIMUM
- POWER DISSIPATION – 165μW/BIT, TYPICAL
- INPUT LOADING – (−100μA), MAXIMUM
- ON-CHIP ADDRESS DECODING
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS
- FAST PROGRAMMING – 5 SEC., MAXIMUM
- PIN COMPATIBLE TO N8204/N8205 ROMs

APPLICATIONS

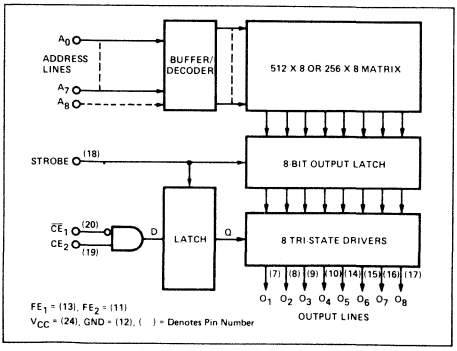
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER		TEST CONDITIONS	LIMITS[1]			UNIT
			MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25	μA
V_{IL}	"0" Level Input Voltage				.85	V
V_{IH}	"1" Level Input Voltage		2 0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6 mA			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE_1}$ = "0", CE_2 = "1", I_{OUT} = −2 mA, "1" STORED	2.7	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 5.5V			40	μA
		$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			−40	μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V, $\overline{CE_1}$ = "1" or CE_2 = 0		8		pF
I_{CC}	V_{CC} Supply Current			135	185	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	mA

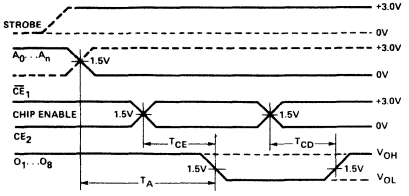
SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60	ns
T_{CE}	Chip Enable Access Time	R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 4)		20	40	ns
T_{CD}	Chip Disable Time			20	40	ns
T_{ADH}	Address Hold Time		0	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		ns
T_{SW}	Strobe Pulse Width	LATCHED READ ONLY	30	20		ns
T_{SL}	Strobe Latch Time	R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 5)	60	35		ns
T_{DL}	Strobe Delatch Time				30	ns
T_{CDS}	Chip Enable Set-up Time		40			ns

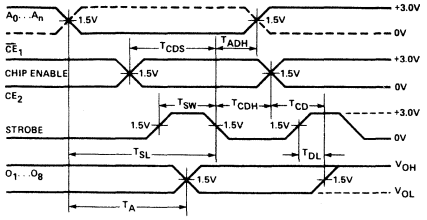
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

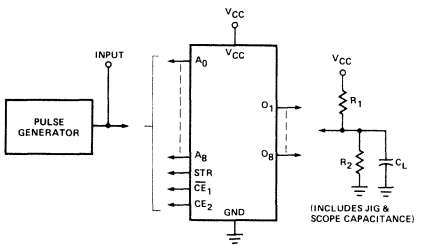
TRANSPARENT READ[5]
(Output Latches Not Used)

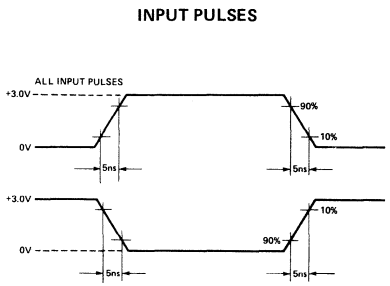


LATCHED READ[6]
(Output Latches Used)

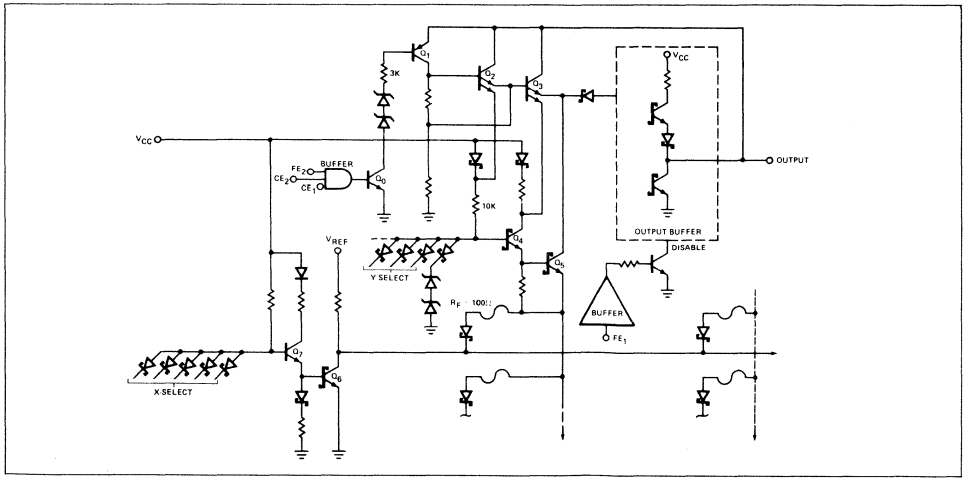


AC TEST LOAD AND WAVEFORMS





TYPICAL FUSING PATH



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 200 ± 25 mA (Transient or steady state)	4.75	5.0	5.25	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +5.0 ± .25V	175	200	225	mA
Input Voltage						
V_{IL}	Low Level Input Voltage		0	0.4	0.8	V
V_{IH}	High Level Input Voltage		2.4		5.5	V
Input Current (FE_1 & FE_2 Only)						
I_{IL}	Low Level Input Current	V_{IL} = +0.45V			-100	μA
I_{IH}	High Level Input Current	V_{IH} = +5.5V			10	mA
Input Current (Except FE_1 & FE_2)						
I_{IL}	Low Level Input Current	V_{IL} = +0.45V			-100	μA
I_{IH}	High Level Input Current	V_{IH} = +5.5V			25	μA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 200 ± 20 mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	FE_2 Programming Pulse Width		1		1.5	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	V_{CC} = V_{CCP}			10	sec
T_{PS}	Programming Pause	V_{CC} = 0V	7			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				60	%

NOTES:
1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 3 mS.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10KΩ resistor to V_{CC}.

c. Set $\overline{CE}$ 1 to logic "0", and CE2 to logic "1" (TTL levels).

d. Set Strobe to logic "1" level.

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to FE1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10 mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit of 200 mA. Program one output at the time.

Step 4 After 10μs delay, raise FE2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10 mA sourcing current capability.

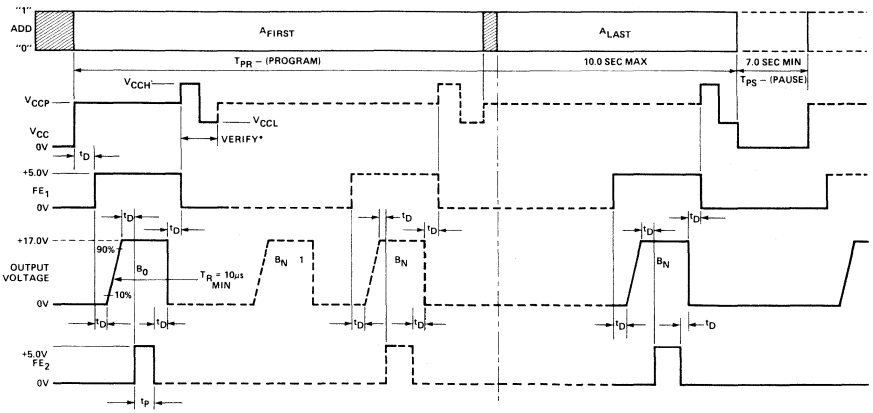
Step 5 After 10μs delay, remove +17.0V supply from programmed output.

Step 6 To verify programming, after 10μs delay, return FE1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.

Step 7 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 6 to program other bits at the same address.

Step 8 Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

signetics

BIPOLAR FIELD-PROGRAMMABLE LOGIC ARRAY (16X8X48 FPLA) 82S101 (OPEN COLLECTOR) 82S100 (TRI-STATE)

82S100 82S101

OBJECTIVE SPECIFICATION

APRIL 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S100 (Tri-State Outputs) and the 82S101 (Open Collector Outputs) are Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 output functions. Each output function can be programmed either true active-High (Fp), or true active-Low ($F\overline{p}^*$). The true state of the output functions is controlled via an output Sum (OR) Matrix by a logical combination of 16-input variables, or their complements, up to 48 terms.

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include a chip-enable clocking input for output deskewing and inhibit. They feature either Open Collector or Tri-State outputs for ease of expansion of product terms and/or input variables.

FEATURES

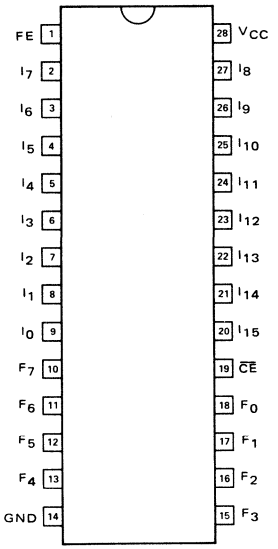
- FIELD PROGRAMMABLE (Ni-Cr LINK)
- INPUT VARIABLES – 16
- OUTPUT FUNCTIONS – 8
- PRODUCT TERMS – 48
- ADDRESS ACCESS TIME – 50ns, MAXIMUM
- POWER DISSIPATION – 600mW, TYPICAL
- INPUT LOADING – (–100μA), MAXIMUM
- OUTPUT OPTION:
  TRI-STATE OUTPUTS – 82S100
  OPEN COLLECTOR OUTPUTS – 82S101
- OUTPUT DISABLE FUNCTION:
  TRI-STATE – Hi-Z
  OPEN COLLECTOR – Hi
- CERAMIC DIP

APPLICATIONS

LARGE READ ONLY MEMORY
RANDOM LOGIC
CODE CONVERSION
PERIPHERAL CONTROLLERS
LOOK-UP AND DECISION TABLES
MICROPROGRAMMING
ADDRESS MAPPING
CHARACTER GENERATORS
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION

I PACKAGE



TRUTH TABLE

LET:

$P_n = \Pi_0^{15} (k_m I_m + j_m \overline{I_m})$; k = 0, 1, X (Don't Care)

n = 0, 1, 2, ... , 47

where:

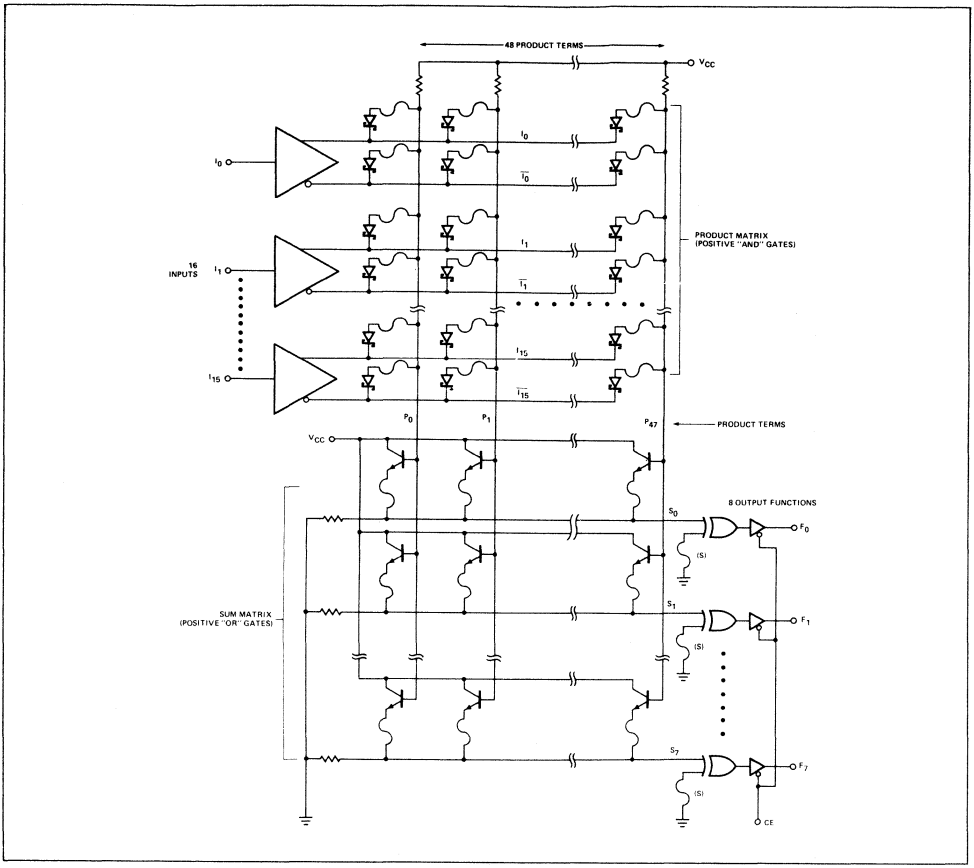
Unprogrammed state : $j_m = k_m = 0$

Programmed state : $j_m = \overline{k_m}$

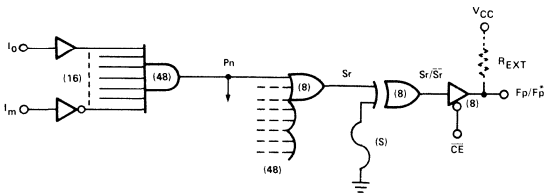
$S_r = f(\Sigma_0^{47} P_n)$; r ≡ p = 0, 1, 2, ... , 7

MODE	P_n	$\overline{CE}$	F_p	F_p^*	$S_r \triangleq f(P_n)$
Disabled (82S101)	X	1	1	1	X
Disabled (82S100)			Hi-Z	Hi-Z	
Read	1	0	1	0	YES
	0	0	0	1	
	X	0	0	1	NO

BLOCK DIAGRAM



FPLA TYPICAL LOGIC PATH



NOTE:
FOR EACH OF THE 8 OUTPUTS, EITHER THE FUNCTION Fp (ACTIVE HIGH) OR Fp (ACTIVE LOW) IS AVAILABLE, BUT NOT BOTH. THE REQUIRED FUNCTION POLARITY IS USER PROGRAMMABLE VIA FUSE (S).

$Pn = I_0 \overline{I_1}\,\overline{I_2}\, I_3 \ldots\ldots \overline{I_m}$

$Sr = P_0 + P_1 + P_2 + \ldots\ldots Pn$

$\overline{Sr} = P_0 \bullet \overline{P_1} \bullet \overline{P_2} \bullet \ldots\ldots \overline{Pn}$

$Fp = (\overline{CE}) + (Sr) = (\overline{CE}) + (P_0 + P_1 + P_2 + \ldots\ldots Pn)$ @ S = SHORT

$\overset{*}{Fp} = (\overline{CE}) + (\overline{Sr}) = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2} \bullet \ldots\ldots \overline{Pn})$ @ S = OPEN

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S101)	+5.5	Vdc
V_O	Off-State Output Voltage (82S100)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

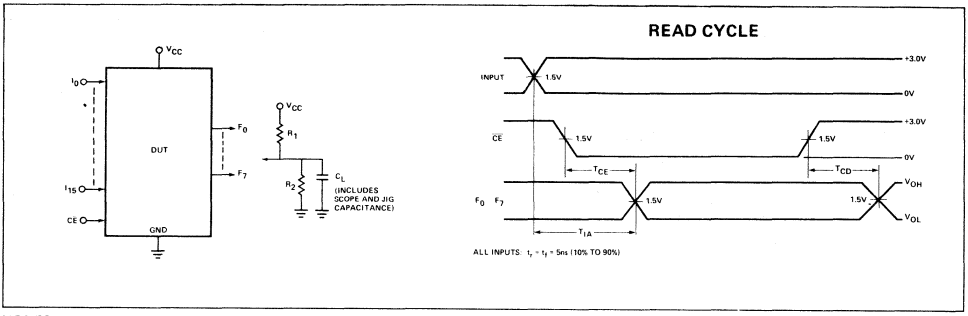
PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT	NOTES
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.8	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −18mA			−0.8	−1.2	V	1, 7
V_{OH}	High-Level Output Voltage (82S100)	V_{CC} = 4.75V, I_{OH} = −2mA		2.4			V	1, 5
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 9.6mA			0.35	0.45	V	1, 8
I_{OLK}	Output Leakage Current (82S101)	V_{CC} = 5.25V	V_{OUT} = 5.25V		1	40	μA	6
$I_{O(OFF)}$	Hi-Z State Output Current (82S100)		V_{OUT} = 5.25V		1	40	μA	6
			V_{OUT} = 0.45V		−1	−40	μA	6
I_{IH}	High-Level Input Current	V_{IN} = 5.5V			<1	25	μA	
I_{IL}	Low-Level Input Current	V_{IN} = 0.45V			−10	−100	μA	
I_{OS}	Short-Circuit Output Current (82S100)	V_{CC} = 5.25V, V_{OUT} = 0V		−20		−70	mA	3, 7
I_{CC}	V_{CC} Supply Current (82S100, 82S101)	V_{CC} = 5.25V			120	170	mA	4
C_{IN}	Input Capacitance	V_{CC} = 5.0V	V_{IN} = 2.0V		5		pF	
C_O	Output Capacitance		V_{OUT} = 2.0V		8		pF	6

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of short circuit should not exceed one second.
4. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each output one at the time.
8. Measured with a programmed logic condition for which the output under test is at a "0" logic level. Output sink current is supplied thru a resistor to V_{CC}.

SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{IA}	Input to Output	C_L = 30pF		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600		15	20	ns

AC TEST FIGURE AND WAVEFORM



NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, and T_A = +25°C.

OBJECTIVE PROGRAMMING PROCEDURE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

A. All internal Ni-Cr links are intact.

B. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "FALSE").

C. The Sum Matrix contains all 48 P-terms.

D. The polarity of each output is set to active HIGH (F_p function).

E. All outputs are at a LOW logic level.

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the Product Matrix, Sum Matrix, and Output Polarity outlined below.

OUTPUT POLARITY

PROGRAM ACTIVE LOW (F_p^* Function)

Program output polarity before programming Product Matrix and Sum Matrix. Program one output at the time.

1. Set GND (pin 14) to OV.
2. Do not apply power to the device (V_{CC}, pin 28, open).
3. Apply V_{OUT} = +18V to the appropriate output for 1ms, and return to OV.
4. Repeat step 3 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to LOW logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a HIGH logic level are programmed active HIGH (F_p function), while all outputs at a LOW logic level are programmed active LOW (F_p^* function).
5. Remove V_{IN} = +10V from inputs I_0 through I_{15}.

PRODUCT MATRIX

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to HIGH logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to

outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage to I_0 from V_{IN} = +10V to a LOW logic level. Execute step 6.

6a. After 10μs delay, raise FE (pin 1) from 0V to +17V. The source must have a current limit of 250mA, and rise time of 10 to 50μs.

6b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

6c. After 10μs delay, return FE input to 0V.

7. Return input I_0 to a disable state by applying V_{IN} = +10V.

8. Repeat steps 5 through 7 for all other input variables.

9. Repeat steps 4 through 8 for all other P-terms.

10. Remove V_{IN} = +10V from all input variables.

VERIFY INPUT VARIABLE

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.

2. Enable F_7 output by setting $\overline{CE}$ to +10V.

3. Disable input variables by applying V_{IN} = +10V to inputs I_0 through I_{15}.

4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to outputs F_0 through F_5.

5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level, and sense the state of output F_7.
   B. Lower the input voltage to I_0 from a HIGH to a LOW logic level, and sense the logic state of output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	Input Variable State Contained In P-Term
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Dont Care
0 1	0 0	$(I_0), (\overline{I_0})$

Note that two tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Return input I_0 to a disable state by applying V_{IN} = +10V.

7. Repeat steps 5 and 6 for all other input variables.

8. Repeat steps 4 through 7 for all other P-terms.

9. Remove V_{IN} = +10V from all input variables.

SUM MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links of unused P-terms in the Sum Matrix are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Disable the chip by setting $\overline{CE}$ (pin 19) to a HIGH logic level.

3. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB. Use standard TTL levels.

4a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $F_0^* = 0$), go to step 6.

4b. If the P-term **is not** contained in output function F_0 ($F_0 = 0$ or $F_0^* = 1$), set to fuse the P_n link by applying V_{OUT} = +10V to output F_0.

5a. After 10μs delay, raise FE (pin 1) from 0V to +17V.

5b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

5c. After 10μs delay, return FE input to 0V.

6. Repeat steps 4 and 5 for all other output functions.

7. Repeat steps 3 through 6 for all other P-terms.

8. Remove +8.5V from V_{CC}.

VERIFY PRODUCT TERM

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Enable the chip by setting $\overline{CE}$ (pin 19) to a LOW logic level.

3. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as the LSB. Use standard TTL levels.

4. To determine the status of the P_n link in the Sum Matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

Output		P-term Link
Active HIGH (F_p)	Active LOW (F_p^*)	
0	1	FUSED
1	0	PRESENT

5. Repeat steps 3 and 4 for all other P-terms.

6. Remove +8.5V from V_{CC}.

16 X 48 X 8 FPLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV _____ DATE _____

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	$\overline{T}_m$	DON'T CARE	PROD. TERM PRESENT IN F_p	PROD. TERM *NOT* PRESENT IN F_p	ACTIVE HIGH	ACTIVE LOW
H	L	X	A	–	H	L
NOTE: All unused inputs must be programmed as DON'T CARE.			NOTE: Output Function entries are independent of programmed output polarity		NOTE: Output Polarity Programmed once only.	

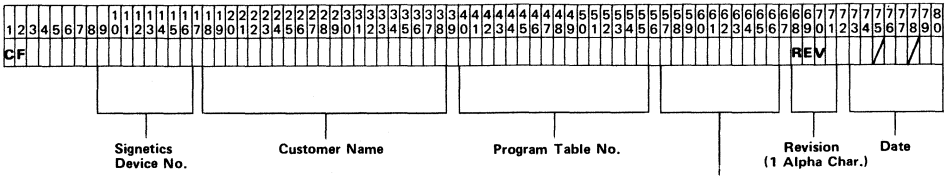
PRODUCT TERM*																	ACTIVE LEVEL							
	INPUT VARIABLE (I_m)																							
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OUTPUT FUNCTION 7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
4																								
5																								
6																								
7																								
8																								
9																								
10																								
11																								
12																								
13																								
14																								
15																								
16																								
17																								
18																								
19																								
20																								
21																								
22																								
23																								
24																								
25																								
26																								
27																								
28																								
29																								
30																								
31																								
32																								
33																								
34																								
35																								
36																								
37																								
38																								
39																								
40																								
41																								
42																								
43																								
44																								
45																								
46																								
47																								

*Both input and output fields of unused P-terms can be left blank.

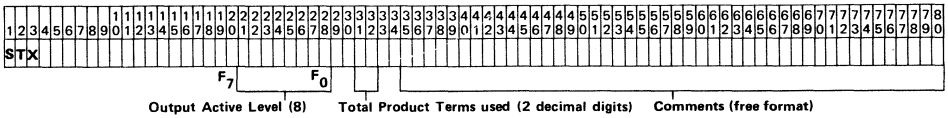
PUNCHED CARD CODING FORMAT

The FPLA Program Table can be supplied directly to Signetics in Punched Card form, using standard 80-column IBM cards. For each FPLA Program Table, the customer should prepare an input card deck in accordance with the following format:

CARD No. 1 - Free format within designated fields.



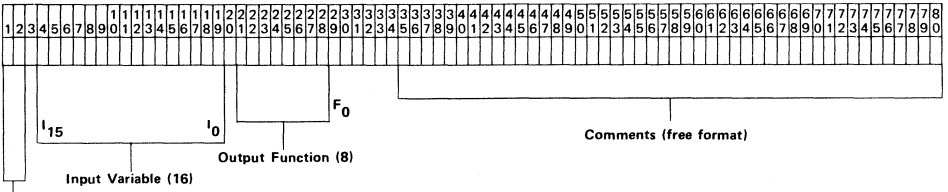
CARD No. 2 -



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
ACTIVE HIGH	ACTIVE LOW
H	L

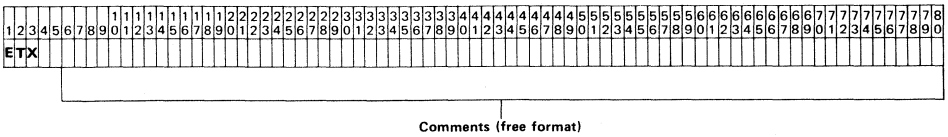
CARD No. 3 through No. 50



Input Variable and Output Function entries are determined in accordance with the following table:

INPUT VARIABLE			OUTPUT FUNCTION	
I_m	I_m	DON'T CARE	PROD. TERM PRESENT IN F_p	PROD. TERM NOT PRESENT IN F_p
H	L	X	A	–
Note: All unused inputs must be programmed as DON'T CARE.			*Note: Output Function entries are independent of programmed output polarity.*	

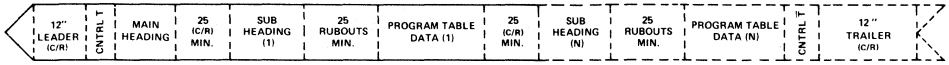
CARD No. 51



Note: Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programmin sequence.

PAPER TAPE CODING FORMAT

The FPLA Program Table can also be sent to Signetics in ASCII tape format via TWX, or air mail using any type of 8-level tape(paper, mylar, fanfold, etc.). A number* of Program Tables can be sequentially assembled on a continuous tape as follows:



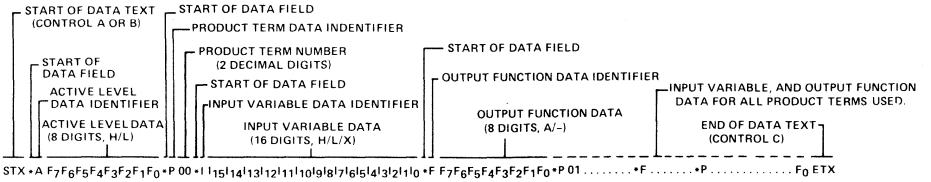
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. **Customer Name**
2. **Customer TWX No.**
3. **Date**
4. **Purchase Order No.**
5. **Number of Program Tables**
6. **Total Number of Parts**

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. **Signetics Device No.**
2. **Program Table No.**
3. **Revision**
4. **Date**
5. **Customer Symbolized Part No.**
6. **Number of Parts**

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information seperated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	I_m	DON'T CARE	PROD. TERM PRESENT, IN F_p	PROD. TERM NOT PRESENT IN F_p	ACTIVE HIGH	ACTIVE LOW
H	L	X	A	–	H	L
Note: All unused inputs must be programmed as DON'T CARE.			*Note: Output Function entries are independent of programmed output polarity*		*Note: Output Polarity programmed once only*	

Although the Product Term data are shown entred in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

Carriage returns, line feeds, and rubout statements may be interspersed between data groups to facilitate an orderly, easily readable teletype printout. This information will be ignored by the programmer during programming. Comments are also allowed between data fields, provided that an asterisk (*) is not used in any heading or comment entry. When correcting or deleting entries, limit consecutive rubouts to less than 25.

* *Limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter.*

signetics

ECL HIGH PERFORMANCE 256-PROM 10139

PRELIMINARY INFORMATION

DIGITAL 10,000 ECL SERIES

DESCRIPTION

The 10139 is an ECL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to low state when the chip enable input is high. This device is fully compatible with all of Signetics series 10,000 products. Address to output access time is 15 ns typical. Power dissipation is 580 milliwatts typical with separate internal bond wires and metal systems for V_{CC1} and V_{CC2}. The 10139 may be programmed to any desired pattern by the user. The 10139 is suitable for use in high performance ECL systems.

TEMPERATURE RANGE

−30 to +85°C Operating Ambient

RECOMMENDED OPERATING VOLTAGE

V_{CC} = GND, V_{EE} = −5.2V ±5%

FEATURES

- **15 ns TYPICAL ACCESS TIME**
- **16 PIN PACKAGE**
- **EASY PROGRAMMING**
- **FULLY DECODED**
- **FULLY COMPATIBLE WITH ECL 10,000 SERIES**
- **HIGH IMPEDANCE INPUTS 50K OHM PULLDOWN**
- **OPEN EMITTER OUTPUTS**

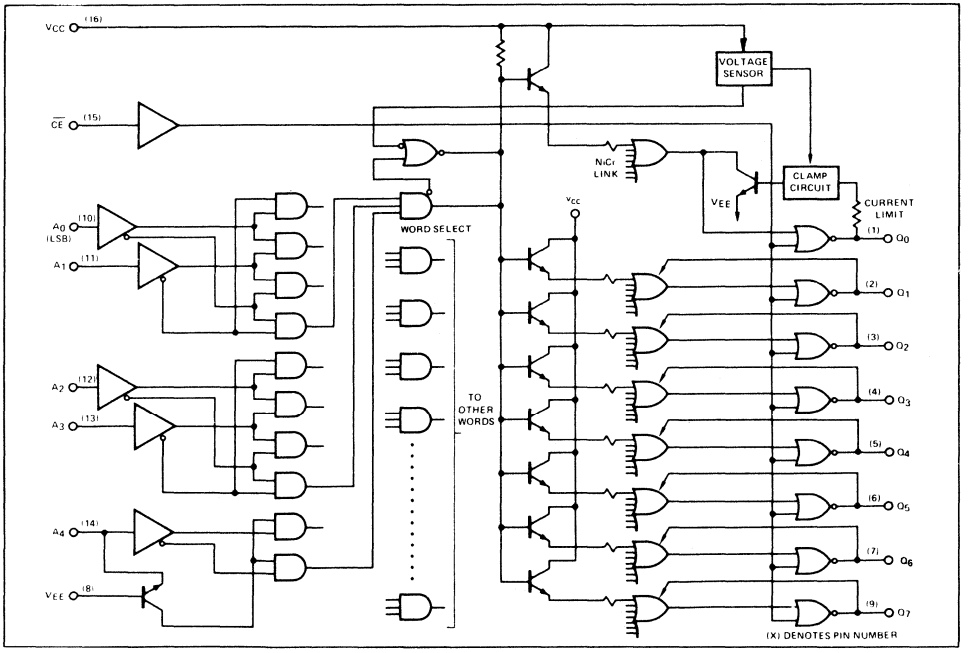
APPLICATIONS

PROGRAMMABLE LOGIC
CONTROL STORES
MICROPROGRAMMING
VOLUME PRODUCTION
HARDWIRED ALGORITHMS

PACKAGE TYPE

F: 16 Pin CERDIP

BLOCK DIAGRAM



PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = OV, R_L = 50Ω, V_{EE} = −5.2V)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Drain Current	I_{EO}		110	145	mAdc
Input Current V_{IH} = −0.810V, V_{IL} = −1.850V	I_{inH} I_{inL}	 30		265	µAdc µAdc
Output Voltage Logic "1" (V_{IH} = −0.810V, V_{IL} = −1.850V)	V_{OH}	−0.960		−0.810	Vdc
Logic "0" (V_{IH} = −0.810V, V_{ILA} = 1.850V)	V_{OL}	−1.990		−1.650	Vdc
Threshold Voltage Logic "1" (V_{IHA} = −1.105V, V_{ILA} = −1.475V)	V_{OHA}	−0.980			Vdc
Logic "0" (V_{IHA} = −1.105V, V_{ILA} = 1.475V)	V_{OLA}			−1.630	Vdc

PRELIMINARY ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = OV, V_{EE} = −5.2V, R_L = 50Ω)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Chip Enable Prop Delay			10	15	ns
Output Rise Time (20 to 80%) Output Fall Time (20 to 80%)			4.2 4.2		ns ns
Access Time Address to Output	T_{AD}		15	20	ns

RECOMMENDED PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write logical "1's", proceed as follows:

MANUAL (see Fig. 1)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Address the word to be programmed by applying 4.0 to 4.6 volts for a logic "1" and 0.0 to 1.0 volts for a logic "0" to the appropriate address inputs.

STEP 2

Raise V_{CC} (Pin 16) to 12 volts.

STEP 3

After V_{CC} has stabilized at 12 volts (including any ringing which may be present on the V_{CC} line) apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

STEP 4

Return V_{CC} to 5.2 volts.

CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 volts for more than 1 second.

STEP 5

Verify that the selected bit has programmed by connecting a 460Ω resistor to ground and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once.

STEP 6

If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (see Fig. 2)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Apply the proper address data and raise V_{CC} (Pin 16) to 12 volts.

STEP 2

After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.5 \leqslant PW \leqslant 1$ ms).

STEP 3

Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time; The delay between output programming pulses should be equal to or less than 1.0 ms.)

STEP 4

After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at 12 volts during the entire programming time.

STEP 5

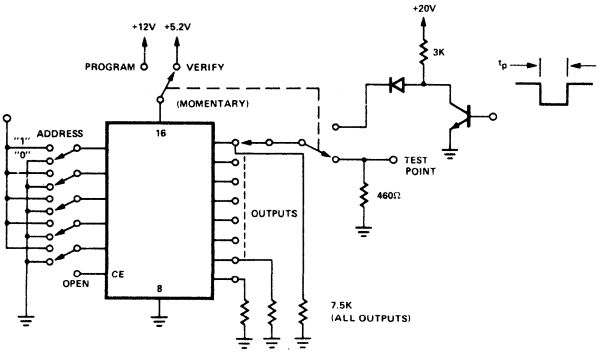
After stepping through all address words, return V_{CC} to +5.2 and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once.

PROGRAMMING SPECIFICATIONS

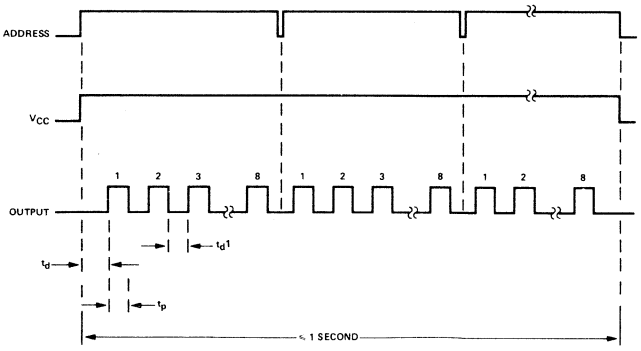
CHARACTERISTIC	SYMBOL	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
Power Supply Voltage						
To Program	V_{CCP}	11.5	12.0	12.5	Volts	
To Verify	V_{CCV}	5.0	5.2	5.4	Volts	
Programming Supply Current	I_{CCP}			250	mA	V_{CC} = 12.0 Volts
Address Voltage						
logical "1"	V_{IH}	4.0		4.6	Volts	
logical "0"	V_{IL}	0.0		1.0	Volts	
Max. Time at $V_{CC} = V_{CCP}$				1.0	Sec.	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mA	
Output Program Pulse Width	t_p	0.5		1.0	ms	
Output Pulse Rise Time				10	μs	
Programming Pulse Delay (1)						
following V_{CC} change	t_d	0.1		1.0	ms	
between output pulses	t_d1	0.01		1.0	ms	

NOTE:
(1) Maximum is specified to minimize the amount of time V_{CC} is at 12 volts.

MANUAL PROGRAMMING CIRCUIT



AUTOMATIC PROGRAMMING CIRCUIT



The requirements for a reliable fusible link SYSTEM can be considered under the following categories:

- Process Control
- Reliability of Unfused Links
- Reliability of Fused Links

PROCESS CONTROLS

Nichrome is used for the fusible link because of the long experience with it as a thin film resistor material. It can be incorporated into the product without any compromises having to be made to the other processing steps.

Ease of fuse control, both geometry and resistance, is greatly improved by use of a "bar" as opposed to "notch" geometry used previously because the alignment of fuse to aluminium leads is much less critical.

As a check of fuse characteristics all wafers are individually measured for fuse width and resistance before being passed to device electrical sort.

The fuses are covered with approximately 1μm of deposited passivation glass ensuring no redeposition of evaporated nichrome in the package following fusing.

RELIABILITY OF UNFUSED LINKS

The main concern with regards to unblown links is the possibility of an unblown link opening under normal circuit operating conditions. All Signetics PROM's are designed such that the link fusing current to operating current ratio is a minimum of 20:1 which ensures low current stress under operating conditions. To verify this, fuse links have been stressed at Signetics at 5 times normal current, at 200°C chip temperature with no failures recorded and a resistance change of less than 2% for a total of 2 million fuse hours (1080 fuses for 2016 hours).

RELIABILITY OF BLOWN LINKS

As fusing current through a nichrome fuse is increased a discontinuity in fusing time is observed. This discontinuity is seen as a sudden decrease in fusing time (from milliseconds to microseconds) for a relatively small change in current. The current density through the fuse at this point (Jcrit) is approximately 2×10^7 Amps/cm^2. The fusing behaviour of the fuses above and below Jcrit is very different and so is the tendency towards fuse regrowth.

For current densities below Jcrit, fusing is thought to be a local oxidation phenomenon. After fusing, the nichrome is seen to have small separation gaps with a distinctive "whisker" shape characteristic. Fuses blown under these conditions have been observed to exhibit regrowth under applied bias.

For current densities above Jcrit, the fusing behaviour is believed to be a very fast melting with surface tension pulling back material from the centre of the fuse. Fuses programmed to these conditions exhibit a distinctively clean separation of the link.

All Signetics PROM circuits are now designed to supply a minimum current density of 4×10^7 Amps/cm^2 to the fuses during programming. Because of these design techniques, Signetics PROM fuses program extremely fast and cleanly. Typical fusing times range from 0.3 to 2 microseconds.

LIFE TEST RESULTS – APRIL 1975

Following the completion of 18,290,000 equivalent device hours at 25°C, consisting of 9.088×10^9 equivalent fused link hours and 9.227×10^9 equivalent unfused link hours there have to the above date been zero link or device failures. This indicates the following Failure Rates and Mean Times Between Failure.

	Failure Rate	M.T.B.F.
DEVICE	.005%/khrs	2×10^7 Hours
FUSED LINK	.00001%/khrs	9.4×10^9 Hours
UNFUSED LINK	.00001%/khrs	9.4×10^9 Hours

These figures are quoted for 60% confidence level at 25°C.

Additional information may be obtained by requesting "Signetics PROM Reliability" Booklet and/or "Signetics TTL PROM Failure Rate Summary – April 1975" from your local Signetics Sales Office.

PROGRAMMERS CURRENTLY ADVERTISED

Although Signetics works very closely with manufacturers of commercially available programming equipment and approves each design of Signetics modules, we cannot guarantee individual programming systems and/or modules, since they are subject to calibration drift and other malfunctions common to all equipment of this type. Since normal programming yield using this equipment is in excess of 90%, any time yield drops substantially below this figure on a large sample of devices (e.g. $<$ 85% on 100 devices), the proper action is to check the particular programming system being used and if everything appears correct, call Signetics for further information.

signetics

1024-BIT BIPOLAR READ ONLY MEMORY (256x4 ROM)

82S226
82S229

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S226 (Open Collector Outputs) and the 82S229 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both the 82S226 and 82S229 are also fully compatible with the 82S126/129, Signetics' 1024-Bit Programmable Read Only Memories.

Both 82S226 and 82S229 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S226/229, B or F. For the military temperature range (−55°C to +125°C) specify S82S226/229, F only.

FEATURES

- **ORGANIZATION – 256 X 4**
- **ADDRESS ACCESS TIME:**
  S82S226/229 – 70ns, MAXIMUM
  N82S226/229 – 50ns, MAXIMUM
- **POWER DISSIPATION – 0.5mW/BIT, TYPICAL**
- **INPUT LOADING:**
  S82S226/229 – (−150μA) MAXIMUM
  N82S226/229 – (−100μA) MAXIMUM
- **TWO CHIP ENABLE INPUTS**
- **ON-CHIP ADDRESS DECODING**
- **OUTPUT OPTIONS:**
  82S226 – OPEN COLLECTOR
  82S229 – TRI-STATE
- **16-PIN CERAMIC PACKAGE**
- **FULLY COMPATIBLE WITH 82S126/129, SIGNETICS' 256 X 4 PROM**

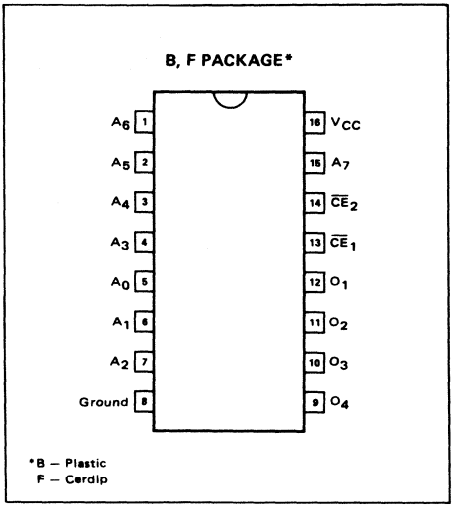
APPLICATIONS

VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

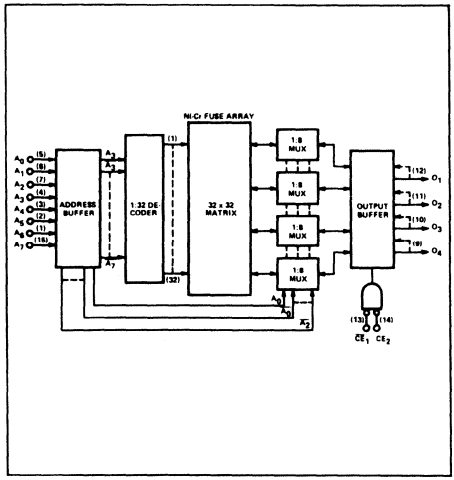
ORDERING INFORMATION

Customer may specify patterns for the 1024-Bit Read Only Memory by completing the truth table/order blank in Signetics'. Truth Table Booklet or by supplying Punched Cards (p.51).

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S226)	+5.5	Vdc
V_O	Off-State Output Voltage (82S229)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S226/229)	0° to +75°	°C
	(S82S226/229)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S226/229 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S226/229 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS[1]	S82S226/229			N82S226/229			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage				.80			.85	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_{IC}	Input Clamp Voltage	$I_{IN} = -18mA$		−0.8	−1.2		−0.8	−1.2	V
V_{OL}	Low Level Output Voltage	$I_{OUT} = 16mA$			0.5			0.5	V
V_{OH}	High Level Output Voltage (82S229)	$\overline{CE}_1 = \overline{CE}_2 =$ "0", $I_{OUT} = -2mA$, "1" STORED	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S226)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", $V_{OUT} = 5.5V$			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S229)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", $V_{OUT} = 5.5V$			60			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = "1", $V_{OUT} = 0.5V$			−60			−40	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.45V$			−150			−100	μA
I_{IH}	High Level Input Current	$V_{IN} = 5.5V$			50			40	μA
I_{OS}	Output Short Circuit Current (82S229)	$V_{OUT} = 0V$	−15		−85	−20		−70	mA
I_{CC}	V_{CC} Supply Current			105	125		105	120	mA
C_{IN}	Input Capacitance	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5			5		pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$		8			8		pF

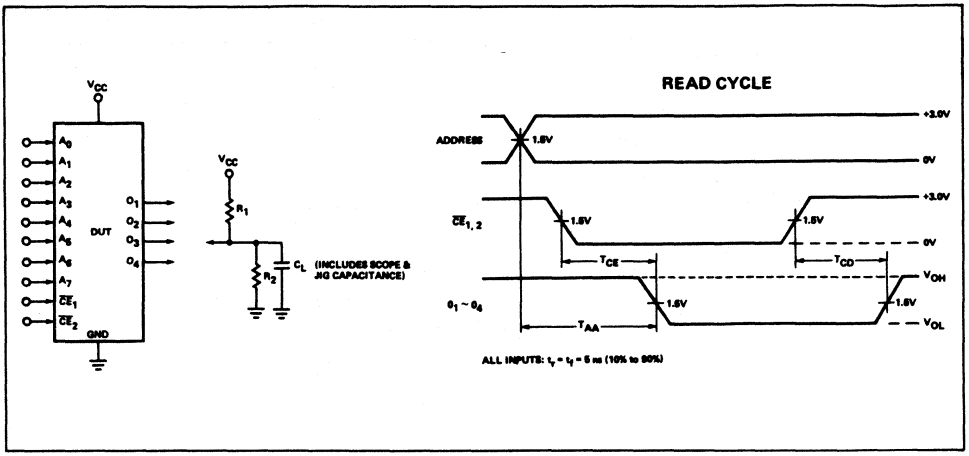
SWITCHING CHARACTERISTICS

S82S226/229 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S226/229 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S226/229			N82S226/229			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	$C_L = 30pF$, $R_1 = 270\Omega$, $R_2 = 600\Omega$		35	70		35	50	ns
T_{CD}	Chip Disable to Output			15	35		15	20	ns
T_{CE}	Chip Enable to Output			15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

AC TEST FIGURE AND WAVEFORM



signetics

2048-BIT BIPOLAR READ-ONLY MEMORY (512x4 ROM)

82S230
82S231

JUNE 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S230 (Open Collector Outputs) and the 82S231 (Tri-State Outputs) are Bipolar 2048-Bit Read Only Memories, organized as 512 words by 4 bits per word. They are fully TTL compatible, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both the 82S230 and 82S231 are also fully compatible with the 82S130/131, Signetics' 2048-Bit Programmable Read Only Memories.

Both 82S230 and 82S231 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S230/231, B or F. For the military temperature range (−55°C to +125°C) specify S82S230/231, F only.

FEATURES

- ORGANIZATION – 512×4
- ADDRESS ACCESS TIME:
  - S82S230/231 – 70ns, MAXIMUM
  - N82S230/231 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT, TYPICAL
- INPUT LOADING:
  - S82S230/231 – (150μA) MAXIMUM
  - N82S230/231 – (100μA) MAXIMUM
- ONE CHIP ENABLE INPUT
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  - 82S230 – OPEN COLLECTOR
  - 82S231 – TRI-STATE
- 16-PIN CERAMIC PACKAGE
- FULLY COMPATIBLE WITH 82S130/131, SIGNETICS' 512 × 4 PROM

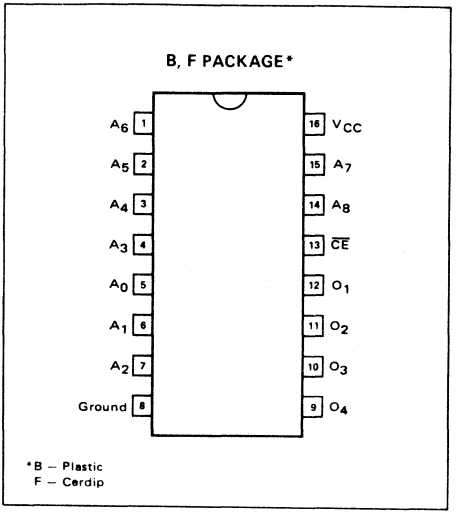
APPLICATIONS

VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

ORDERING INFORMATION

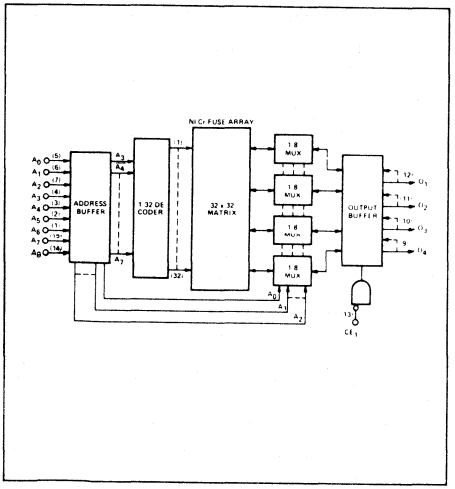
Customer may specify patterns for the 2048 Bit Read Only Memory by completing the truth table/order blank in Signetics'. Truth Table Booklet or by supplying Punched Cards (p.51).

PIN CONFIGURATION



*B – Plastic
F – Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S230)	+5.5	Vdc
V_O	Off-State Output Voltage (82S231)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S230/131)	0° to +75°	°C
	(S82S230/131)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S230/231 − 55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
N82S230/231 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER		TEST CONDITIONS[1]	S82S226/229			N82S226/229			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage				.80			.85	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
V_{OL}	Low Level Output Voltage	I_{OUT} = 16mA			0.5			0.5	V
V_{OH}	High Level Output Voltage (82S231)	$\overline{CE}$ = "0", I_{OUT} = −2mA, "1" STORED	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S230)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			60			40	µA
$I_{O(OFF)}$	Hi-Z State Output Current (82S231)	$\overline{CE}$ = "1", V_{OUT} = 5.5V			60			40	µA
		$\overline{CE}$ = "1", V_{OUT} = 0.5V			−60			−40	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V			−150			−100	µA
I_{IH}	High Level Input Current	V_{IN} = 5.5V			50			40	µA
I_{OS}	Output Short Circuit Current (82S231)	V_{OUT} = 0V	−15		−85	−20		−70	mA
I_{CC}	V_{CC} Supply Current			120	140		120	140	mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		8			8		pF

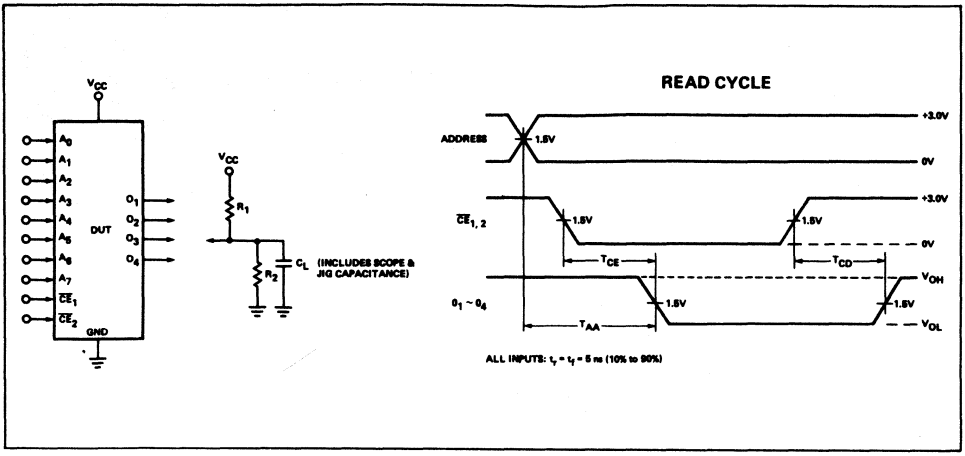
SWITCHING CHARACTERISTICS

S82S230/231 −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
N82S230/231 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	S82S230/231			N82S230/231			UNIT
		MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
Propagation Delay								
T_{AA} Address to Output	C_L = 30pF		35	70		35	50	ns
T_{CD} Chip Disable to Output	R_1 = 270Ω		15	35		15	20	ns
T_{CE} Chip Enable to Output	R_2 = 600Ω		15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

AC TEST FIGURE AND WAVEFORM



signetics

2048-BIT BIPOLAR ROM (256x8 ROM)
4096-BIT BIPOLAR ROM (512x8 ROM)

DIGITAL 8000 SERIES TTL/MEMORY

8204
8205
(82S214)
(82S215)

DESCRIPTION

The 8204/82S214 and 8205/82S215 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers.

The 8204/82S214 and 8205/82S215 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by CE1 and CE2 lines. In the LATCHED READ mode, after the desired address is applied and both CE1 and CE2 are enabled, data will enter the output latches following the positive transition of STROBE, and the data out lines will be locked into their last valid state following the negative transition of STROBE. The latches will remain set and the outputs enabled until the chip is disabled and STROBE is brought high.

Both 8204/82S214 and 8205/82S215 devices are available in the commercial temperature range.

FEATURES

- ORGANIZATION:
  8204/82S214 – 256 × 8
  8205/82S215 – 512 × 8
- ADDRESS ACCESS TIME – 75ns, MAXIMUM
- POWER DISSIPATION – 165μW/BIT, TYPICAL
- INPUT LOADING – (400μA), MAXIMUM
- ON-CHIP ADDRESS DECODING
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS

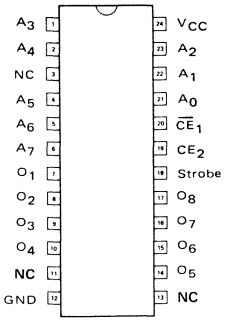
APPLICATIONS

MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

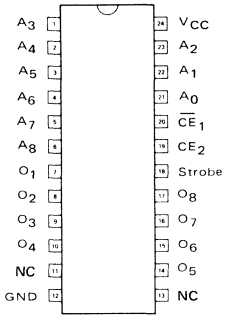
PIN CONFIGURATION

I PACKAGE*

8204/82S214

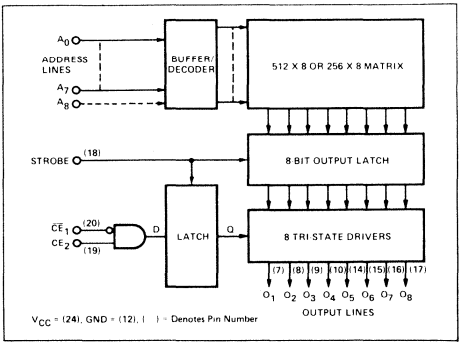


8205/82S215



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	LIMITS[1]			UNIT
			MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			− 400	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25	μA
V_{IL}	"0" Level Input Voltage				85	V
V_{IH}	"1" Level Input Voltage		2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6 mA			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE_1}$ = "0", CE_2 = "1", I_{OUT} = −2 mA, "1" STORED	2.7	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 5.5V $\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			40 −40	μA μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V $\overline{CE_1}$ = "1" or CE_2 = 0		8		pF
I_{CC}	V_{CC} Supply Current			135	170	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	mA

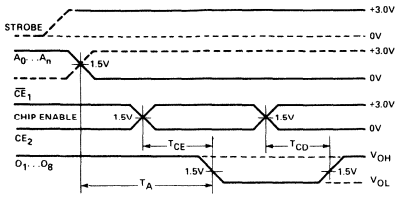
SWITCHING CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	75	ns
T_{CE}	Chip Enable Access Time	R_1 = 470Ω, R_2 = 5KΩ, C_L = 30pF (Note 4)		20	50	ns
T_{CD}	Chip Disable Time			20	50	ns
T_{ADH}	Address Hold Time	LATCHED READ ONLY R_1 = 470Ω, R_2 = 5KΩ, C_L = 30pF (Note 5)	0	−10		ns
T_{CDH}	Chip Enable Hold Time		15	5		ns
T_{SW}	Strobe Pulse Width		35	20		ns
T_{SL}	Strobe Latch Time		75	45		ns
T_{DL}	Strobe Delatch Time			18	35	ns
T_{CDS}	Chip Enable Set-up Time		40			ns

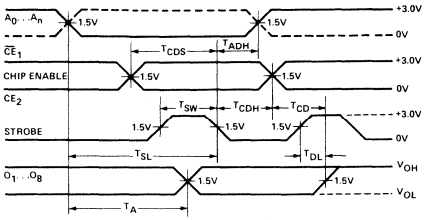
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

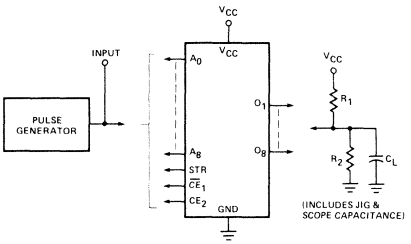
TRANSPARENT READ[5]
(Output Latches Not Used)



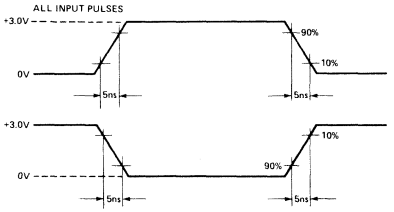
LATCHED READ[6]
(Output Latches Used)



AC TEST LOAD AND WAVEFORMS



INPUT PULSES



signetics

4096 BIT BIPOLAR ROM (1024x4 ROM) 8228

THIS PRODUCT AVAILABLE IN 0°C TO 75°C TEMPERATURE RANGE ONLY

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 8228 is a 4096 Bit Bipolar Read Only Memory organized as 1024 words by 4 bits per word. Available in a 16 pin dual in-line package, the 8228 can provide very high bit packing density by replacing four standard 256×4 ROMS.

The 8228 is fully TTL compatible and includes on-the-chip decoding. Typical access time is 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N82281 - CD162.

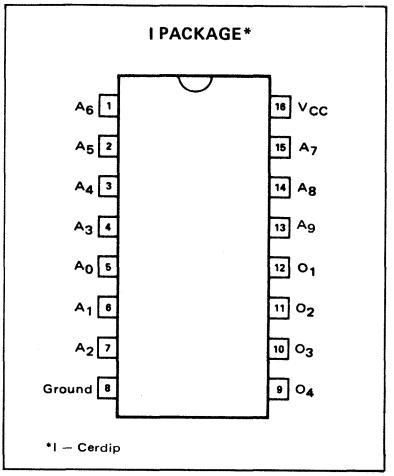
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TOTEM POLE OUTPUTS
- DIODE PROTECTED INPUTS
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)

APPLICATIONS

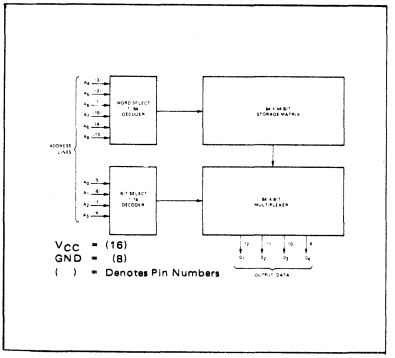
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CHARACTER RECOGNITION
CHARACTER GENERATION
CONTROL STORE

PIN CONFIGUARATION



*I — Cerdip

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			0.5	V	I_{out} = 11.2 mA	
"1" Output Voltage	2.7			V	I_{out} = 1.0 mA	
"0" Input Current		-10	400	A	V_{in} = 0.45V	
"1" Input Current		1	25	A	V_{in} = 5.5V	
Input Threshold Voltage						
"0" Level			85	V		
"1" Level	2.0			V		
Input Clamp Voltage	1.2			V	I_{in} = 13 mA	
Power Consumption		140	170	mA	Θ_1 to Θ_3 = "0"	
Output Short Circuit Current	-20		-70	mA		

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

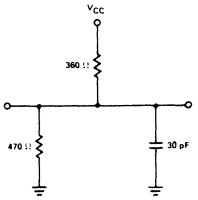
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Access Time—Address to Output		50	70	ns		5

NOTES:

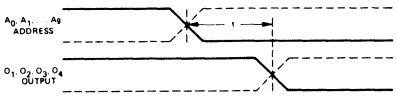
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 5.5V
   Input currents must not exceed +30mA
   Output currents must not exceed +100mA
   Storage temperature must be between -60°C to + 150°C
5. Rise and fall time for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

AC TEST FIGURE AND WAVEFORM

TEST LOAD



READ CYCLE



BIPOLAR ROM CARD FORMATS FOR DEVICES WITH FOUR (4) BITS PER WORD: 82S226/229 82S230/231 8228

CARD 1 (START AND IDENTIFICATION CARD)

COLUMN (1–8) Signetics Part Number (include temperature range prefix and package designator).

(9, 10) Blank.

(11–44) Customer Part Number.

(45, 46) Leave blank.

(47–56) Symbol Required on Package.

(57–80) Leave blank.

CARD 2 THROUGH N (DATA CARDS)

COLUMN (1–4) Decimal Equivalent of Address Zero (0000).

(5) Blank.

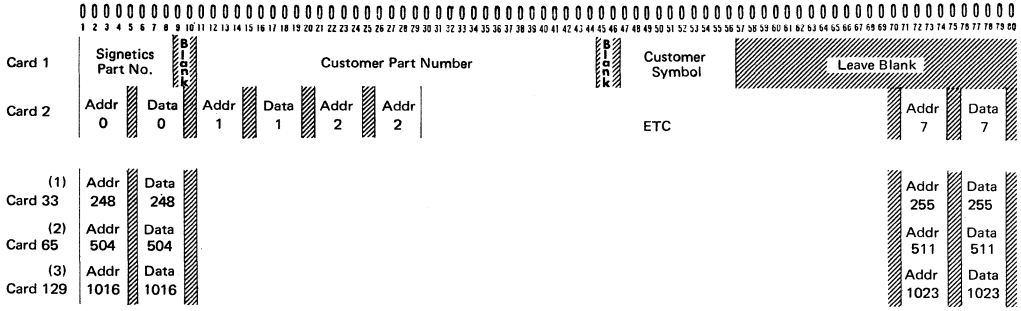
(6–9) Binary Data Output with HSB on the left.

(10) Blank.

(11–14) Decimal Equivalent of Address One (0001).

ETC.

EXAMPLE



NOTES:
1. Last card for 256 x 4 ROM (82S226/229)
2. Last card for 512 x 4 ROM (82S230/231)
3. Last card for 1024 x 4 ROM (8228)
4. "Zero" levels on Data Outputs are defined as Low.
5. Address bit A_0 is the Least Significant Address bit.

FOR DEVICES WITH EIGHT (8) BITS PER WORD: 8204/82S214 8205/82S215

CARD 1 (START AND IDENTIFICATION CARD)

COLUMN (1–8) SIGNETICS Part Number (include temperature range prefix and package designator).

(9, 10) Leave blank.

(11–44) Customer Part Number.

(45, 46) Leave blank.

(47–56) Symbol Required on Package.

(57–80) Leave blank.

CARD 2 THROUGH N (DATA CARDS)

(1–3) Decimal Equivalent of Address Zero (000).

(4) Blank.

(5–12) Binary Data Output with MSB on the left.

(13–20) Blank.

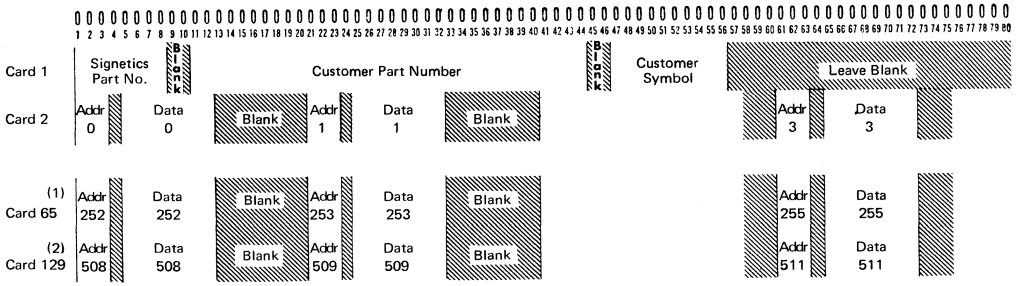
(21–23) Decimal Equivalent of Address One (001).

(24) Blank.

(25–32) Binary Data Output.

ETC.

EXAMPLE



NOTES:
1. Last card for 256 x 8 ROM (8204/82S214)
2. Last card for 512 x 8 ROM (8205/82S215)
3. "Zero" levels on Data Outputs are defined as Low
4. Address bit A_0 is the Least Significant Address bit.

TYPE		CONFIGU-RATION	OUTPUT	MAX ACCESS TIME	SIGNETICS PART NUMBER
TTL	RAM	16 × 4	OC	50ns	82S25
			OC	35ns	3101A
		64 × 9	OC	50ns	82S09
		256 × 1	OC	50ns	82S17
					74S301
				40ns	82S117
			TS	50ns	82S16
					74S201
				40ns	82S116
		1024 × 1	OC	45ns	82S10
					93415A
			TS	45ns	82S11
					93425A
	CAM	4 × 2	OC	20ns†	8220
	WWR	32 × 2	OC	50ns	82S21
	SAM	8 × 4	OC	30ns	82S12
			TS	30ns	82S112
ECL	RAM	16 × 4	OE	13ns	10145
		64 × 1	OE	15ns	10140‡
			OE	10ns	10142
			OE	15ns	10148
		256 × 1	OE	30ns	10144
		1024 × 1	OE	35ns	10146**
	WWR	64 × 1	OE	15ns	10151
	CAM	8 × 2	OE	8ns†	10155**

TYPE		CONFIGU-RATION	MAX ACCESS TIME	PINS	SIGNETICS PART NUMBER
MOS	SRAM	256 × 1	1000	16	2501
					25L01
		1024 × 1	1000	16	2602
					2102
					21L02
			650	16	2602-2
					2102-2
					21L02-2
			500	16	2602-1
					2102-1
					21L02-1
			450	16	21F02-4
			400	16	21L02-3
			350	16	21F02
			250	16	21F02-2
		256 × 4	750	16	2606
			500	16	2606-1
	DRAM	1024 × 1	300	18	1103
			150	18	1103-1
		4096 × 1	300	22	2604
				16	2660
			200	22	2680
				18	2670

† Typical Associate Time

** To be Announced

‡ Specified for Driving 90Ω load

OC = Open Collector

TS = Tri-State

OE = Open-Emitter

For further information on these devices request "SIGNETICS RAM BOOKLET" from your local Sales Office/Distributor.

Signetics

64X8X5 CHARACTER GENERATOR | 2513

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2513 is a high speed 2560-bit Static ROM organized as 64x8x5. A standard 7x5 dot matrix fits well in the 2513. The product uses +5V, -5V and -12V power supplies, TTL level interface signals and Tri-State Outputs for direct, low cost interfacing with TTL, DTL, CMOS and 2500 Series MOS.

FEATURES

- **450 ns TYPICAL ACCESS TIME**
- **STATIC OPERATION**
- **TTL/DTL COMPATIBLE INPUTS**
- **+5, -5, -12V POWER SUPPLIES**
- **TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR BUSSING CAPABILITY**
- **2513/CM2141 ASCII FONT STANDARD(7X5)**
- **24-PIN DIP**
- **P-MOS SILICON GATE TECHNOLOGY**

APPLICATIONS

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' P channel Silicon Gate Process allows the design and production of higher functional density and operating speed than other techniques.

SILICONE PACKAGING

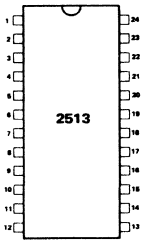
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers.

BIPOLAR COMPATIBILITY

All inputs of the 2513 can be driven directly by standard TTL voltage levels. The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N/I PACKAGE



1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.		15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

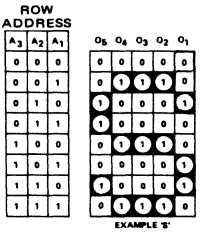
PART IDENTIFICATION TABLE

PART	ORGANIZATION	PROGRAMMING
2513N/I CM2141	64X8X5	ASCII Font
2513N/I CMXXXX	64X7X5 64X8X5	Custom

N PACKAGE = 24 PIN SILICONE DIP

I PACKAGE = 24 PIN CERAMIC DIP

CHARACTER FORMAT



CHARACTER ADDRESS

	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T_A 70°C	730mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

NOTES

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = −5V ±5%; V_{GG} = −12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

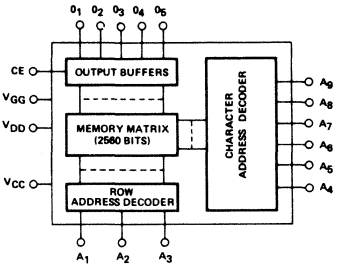
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C $V_{CE} = V_{CC}$
I_{DD}	V_{DD} Power Supply Current		12	15	mA	Outputs Open
I_{GG}	V_{GG} Power Supply Current		10	15	mA	Outputs Open $V_{CE} = V_{CC}$
V_{IL}	Input Logic "0"			+0.6	V	Note 8
V_{IH}	Input Logic "1"	+3.4		5.3	V	Note 8

AC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5V ±5%; V_{DD} = −5V ±5%; V_{GG} = −12V ±5%; unless otherwise noted.

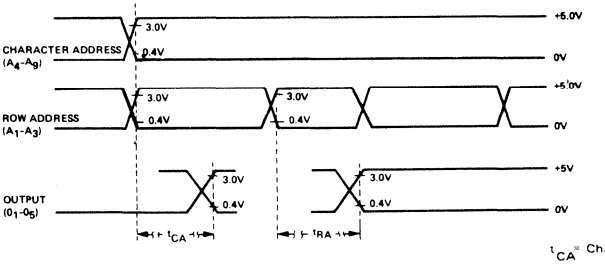
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.4	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
t_{CA}(CM2141)	Character Access Time		500	600	ns	See AC Test Setup
t_{RA}	Row Access Time (A_1 - A_3)		450	500	ns	See AC Test Setup
t_{CE}	Chip Enable to Output		150		ns	
C_{IN}	Address Input Capacitance			10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25mV p - p

BLOCK DIAGRAM



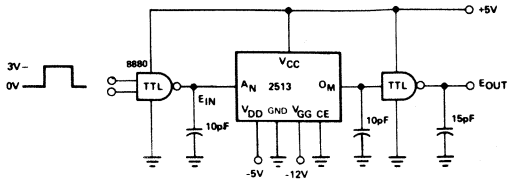
CE	OUTPUT
0	DATA
1	OPEN

TIMING DIAGRAM



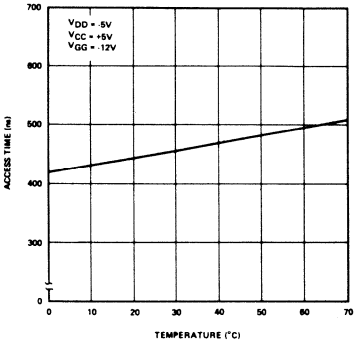
t_{CA} = Character Access Time
t_{RA} = Row Access Time

AC TEST SETUP

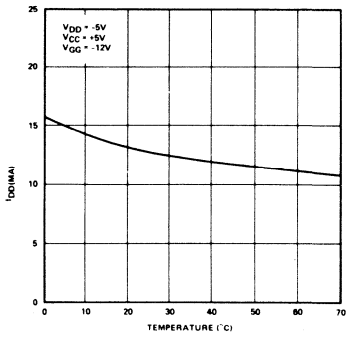


TYPICAL CHARACTERISTIC CURVES

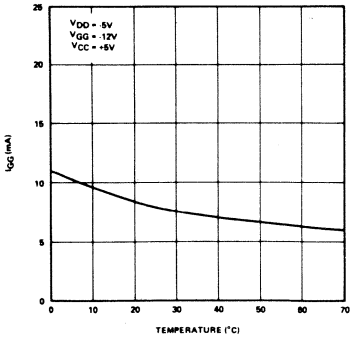
TYPICAL ACCESS TIME VERSUS TEMPERATURE



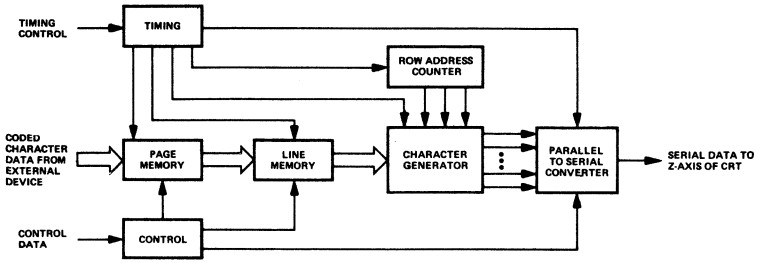
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



APPLICATIONS INFORMATION



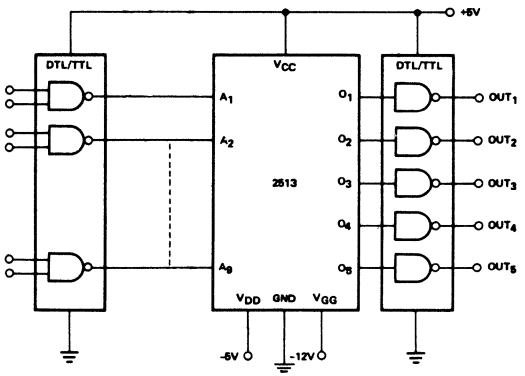
APPLICATION INFORMATION

CHARACTER GENERATOR: The 2513 IS DESIGNED TO PROVIDE THE INFORMATION NEEDED TO CONVERT THE CHARACTER CODES INTO A DOT MATRIX FOR DISPLAY.

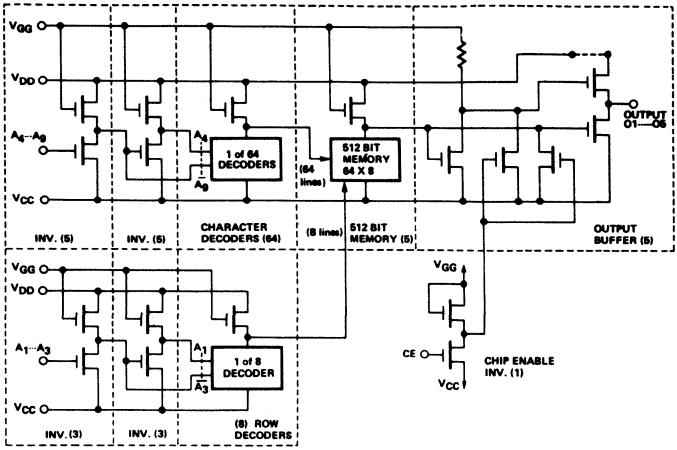
PAGE MEMORY: THIS MEMORY CONTAINS CHARACTER CODES. TYPICALLY, IT CONTAINS THE SAME NUMBER OF CHARACTER CODES AS THE NUMBER OF CHARACTERS ON A FULL SCREEN.

LINE MEMORY: THIS MEMORY CONTAINS THE CHARACTER CODES FOR ONE LINE OF THE CRT DISPLAY.

DTL/TTL INTERFACING

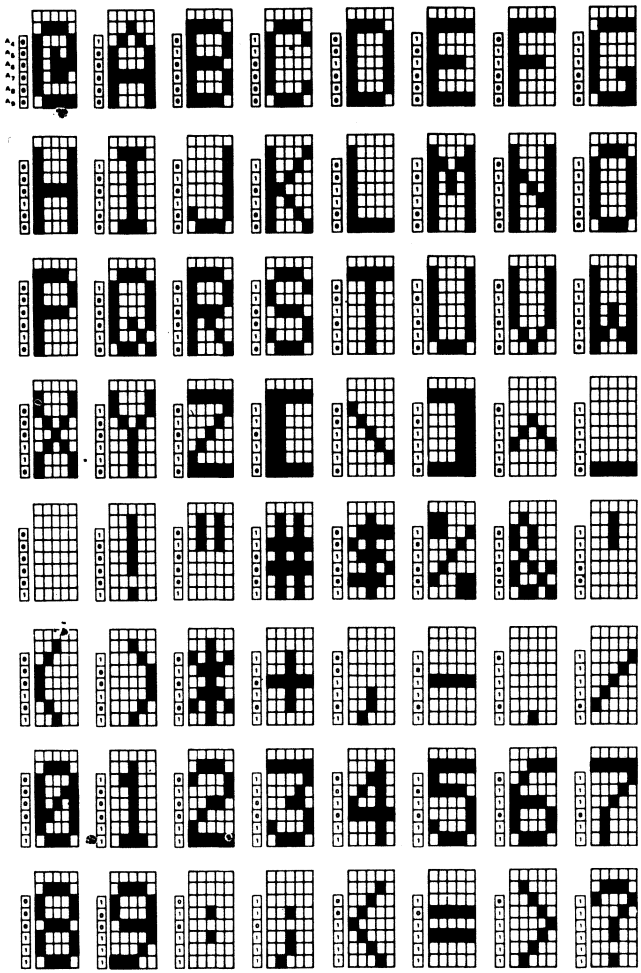


CIRCUIT CROSS-SECTION



ASCII CHARACTER FONT

2513N/CM2141



COMPANY_____

ADDRESS_____

_____

TELEPHONE_____

AUTHORIZED SIGNATURE_____

DATE_____

CUSTOMER PRINT OR ID NO._____

PURCHASE ORDER NUMBER_____

DEVICE TYPE_____ 2513_____

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS)_____

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A three bit binary address code (A_1 through A_3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix. See Figure 1. The devices may also be used in pairs to provide 9 X 7 and 10 X 8 vertical scan formats.

CHARACTER FORMAT

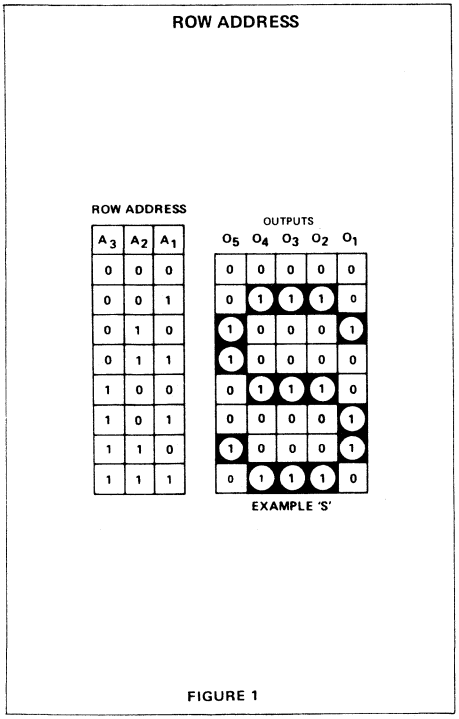


FIGURE 1

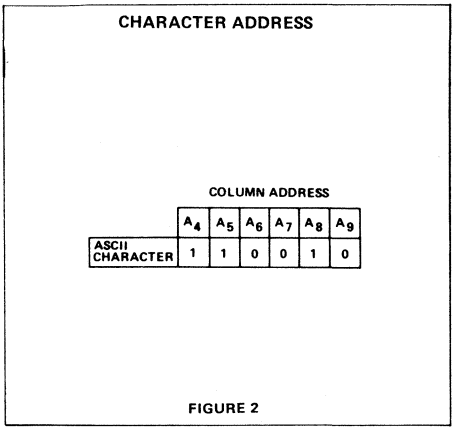


FIGURE 2

ORGANIZATION AS READ-ONLY MEMORY

For a straight 512 X 5 read-only memory, the five outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1 through A_9.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of the basic product type followed by a unique CM number assigned by Signetics. For example, "2513N/CM2141".

- **PROGRAMMING WITH PUNCHED CARDS**
  For maximum accuracy and minimum cost and turnaround time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- **PROGRAMMING WITH WRITTEN TRUTH TABLE**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

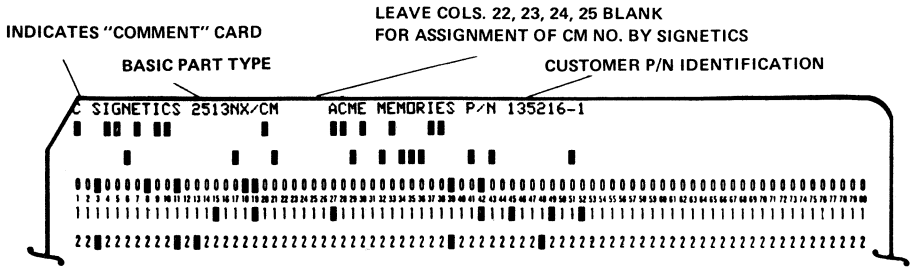
VERIFICATION

Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

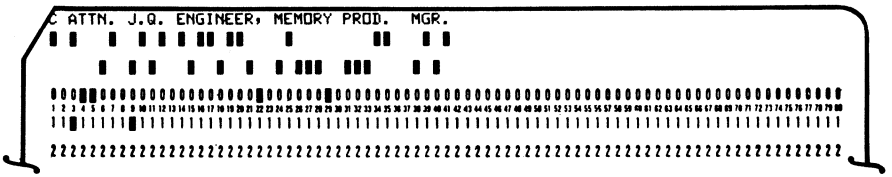
LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. 3.2V minimum). Similarly, a "1" address input level is interpreted as 3.2V minimum.

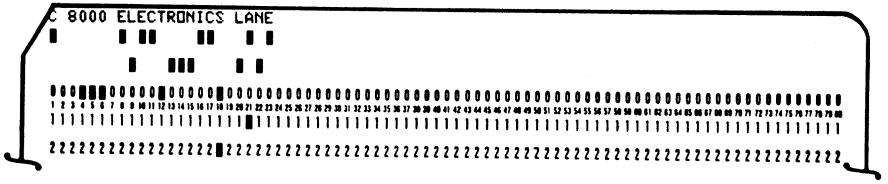
IDENTIFICATION CARDS



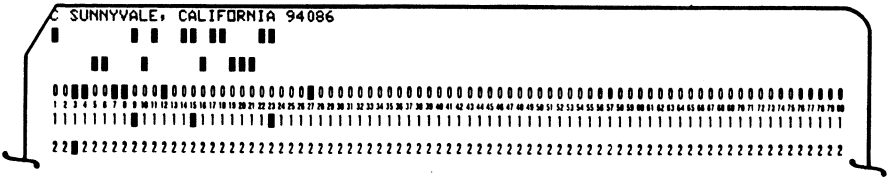
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS
COMPUTER GENERATED TRUTH TABLE



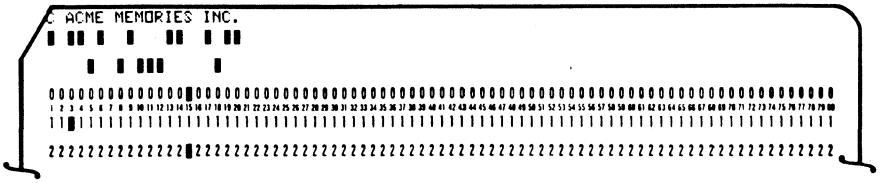
STREET ADDRESS



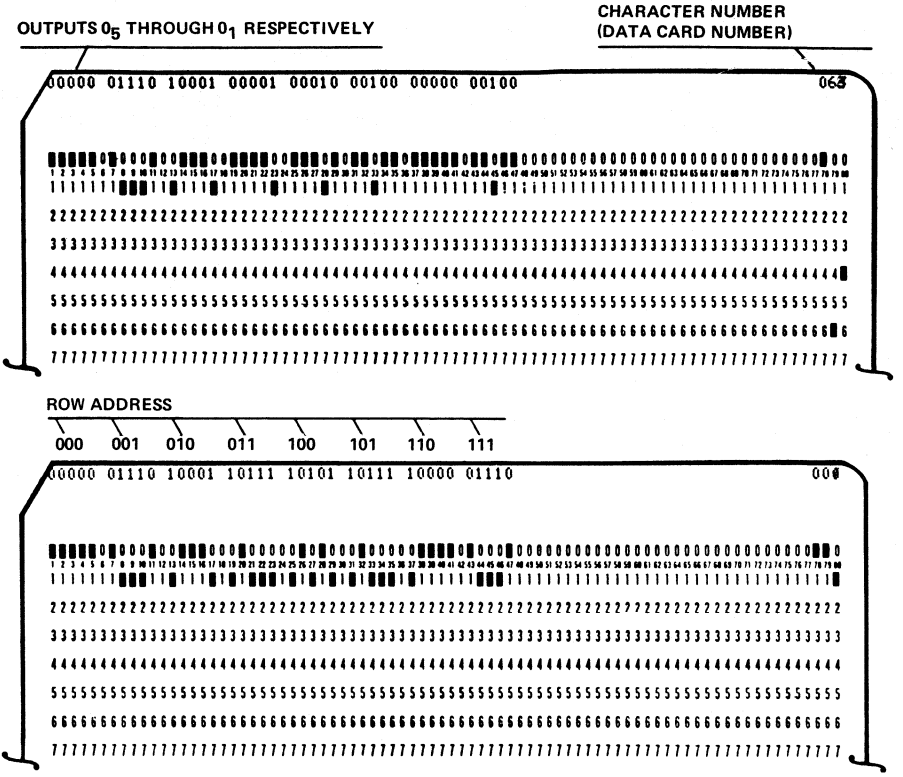
CITY STATE ZIP



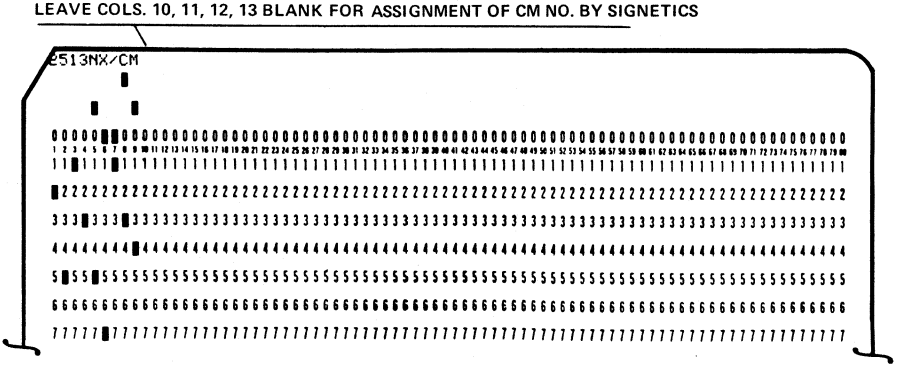
COMPANY NAME



DATA CARDS



BASIC DEVICE TYPE



NOTE:
"Character" number is in columns 78, 79, and 80. Note that each group of eight 5-bit words is treated as a character for convenience of coding.

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 0 0 0 0 0 0 0	000						
0 0 0 0 0 0 0 0 1	001						
0 0 0 0 0 0 0 1 0	002						
0 0 0 0 0 0 0 1 1	003						
0 0 0 0 0 0 1 0 0	004						
0 0 0 0 0 0 1 0 1	005						
0 0 0 0 0 0 1 1 0	006						
0 0 0 0 0 0 1 1 1	007						
0 0 0 0 0 1 0 0 0	008						
0 0 0 0 0 1 0 0 1	009						
0 0 0 0 0 1 0 1 0	010						
0 0 0 0 0 1 0 1 1	011						
0 0 0 0 0 1 1 0 0	012						
0 0 0 0 0 1 1 0 1	013						
0 0 0 0 0 1 1 1 0	014						
0 0 0 0 0 1 1 1 1	015						
0 0 0 0 1 0 0 0 0	016						
0 0 0 0 1 0 0 0 1	017						
0 0 0 0 1 0 0 1 0	018						
0 0 0 0 1 0 0 1 1	019						
0 0 0 0 1 0 1 0 0	020						
0 0 0 0 1 0 1 0 1	021						
0 0 0 0 1 0 1 1 0	022						
0 0 0 0 1 0 1 1 1	023						
0 0 0 0 1 1 0 0 0	024						
0 0 0 0 1 1 0 0 1	025						
0 0 0 0 1 1 0 1 0	026						
0 0 0 0 1 1 0 1 1	027						
0 0 0 0 1 1 1 0 0	028						
0 0 0 0 1 1 1 0 1	029						
0 0 0 0 1 1 1 1 0	030						
0 0 0 0 1 1 1 1 1	031						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 0 1 0 0 0 0 0	032						
0 0 0 1 0 0 0 0 1	033						
0 0 0 1 0 0 0 1 0	034						
0 0 0 1 0 0 0 1 1	035						
0 0 0 1 0 0 1 0 0	036						
0 0 0 1 0 0 1 0 1	037						
0 0 0 1 0 0 1 1 0	038						
0 0 0 1 0 0 1 1 1	039						
0 0 0 1 0 1 0 0 0	040						
0 0 0 1 0 1 0 0 1	041						
0 0 0 1 0 1 0 1 0	042						
0 0 0 1 0 1 0 1 1	043						
0 0 0 1 0 1 1 0 0	044						
0 0 0 1 0 1 1 0 1	045						
0 0 0 1 0 1 1 1 0	046						
0 0 0 1 0 1 1 1 1	047						
0 0 0 1 1 0 0 0 0	048						
0 0 0 1 1 0 0 0 1	049						
0 0 0 1 1 0 0 1 0	050						
0 0 0 1 1 0 0 1 1	051						
0 0 0 1 1 0 1 0 0	052						
0 0 0 1 1 0 1 0 1	053						
0 0 0 1 1 0 1 1 0	054						
0 0 0 1 1 0 1 1 1	055						
0 0 0 1 1 1 0 0 0	056						
0 0 0 1 1 1 0 0 1	057						
0 0 0 1 1 1 0 1 0	058						
0 0 0 1 1 1 0 1 1	059						
0 0 0 1 1 1 1 0 0	060						
0 0 0 1 1 1 1 0 1	061						
0 0 0 1 1 1 1 1 0	062						
0 0 0 1 1 1 1 1 1	063						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 1 0 0 0 0 0 0	064						
0 0 1 0 0 0 0 0 1	065						
0 0 1 0 0 0 0 1 0	066						
0 0 1 0 0 0 0 1 1	067						
0 0 1 0 0 0 1 0 0	068						
0 0 1 0 0 0 1 0 1	069						
0 0 1 0 0 0 1 1 0	070						
0 0 1 0 0 0 1 1 1	071						
0 0 1 0 0 1 0 0 0	072						
0 0 1 0 0 1 0 0 1	073						
0 0 1 0 0 1 0 1 0	074						
0 0 1 0 0 1 0 1 1	075						
0 0 1 0 0 1 1 0 0	076						
0 0 1 0 0 1 1 0 1	077						
0 0 1 0 0 1 1 1 0	078						
0 0 1 0 0 1 1 1 1	079						
0 0 1 0 1 0 0 0 0	080						
0 0 1 0 1 0 0 0 1	081						
0 0 1 0 1 0 0 1 0	082						
0 0 1 0 1 0 0 1 1	083						
0 0 1 0 1 0 1 0 0	084						
0 0 1 0 1 0 1 0 1	085						
0 0 1 0 1 0 1 1 0	086						
0 0 1 0 1 0 1 1 1	087						
0 0 1 0 1 1 0 0 0	088						
0 0 1 0 1 1 0 0 1	089						
0 0 1 0 1 1 0 1 0	090						
0 0 1 0 1 1 0 1 1	091						
0 0 1 0 1 1 1 0 0	092						
0 0 1 0 1 1 1 0 1	093						
0 0 1 0 1 1 1 1 0	094						
0 0 1 0 1 1 1 1 1	095						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 0 1 1 0 0 0 0 0	096						
0 0 1 1 0 0 0 0 1	097						
0 0 1 1 0 0 0 1 0	098						
0 0 1 1 0 0 0 1 1	099						
0 0 1 1 0 0 1 0 0	100						
0 0 1 1 0 0 1 0 1	101						
0 0 1 1 0 0 1 1 0	102						
0 0 1 1 0 0 1 1 1	103						
0 0 1 1 0 1 0 0 0	104						
0 0 1 1 0 1 0 0 1	105						
0 0 1 1 0 1 0 1 0	106						
0 0 1 1 0 1 0 1 1	107						
0 0 1 1 0 1 1 0 0	108						
0 0 1 1 0 1 1 0 1	109						
0 0 1 1 0 1 1 1 0	110						
0 0 1 1 0 1 1 1 1	111						
0 0 1 1 1 0 0 0 0	112						
0 0 1 1 1 0 0 0 1	113						
0 0 1 1 1 0 0 1 0	114						
0 0 1 1 1 0 0 1 1	115						
0 0 1 1 1 0 1 0 0	116						
0 0 1 1 1 0 1 0 1	117						
0 0 1 1 1 0 1 1 0	118						
0 0 1 1 1 0 1 1 1	119						
0 0 1 1 1 1 0 0 0	120						
0 0 1 1 1 1 0 0 1	121						
0 0 1 1 1 1 0 1 0	122						
0 0 1 1 1 1 0 1 1	123						
0 0 1 1 1 1 1 0 0	124						
0 0 1 1 1 1 1 0 1	125						
0 0 1 1 1 1 1 1 0	126						
0 0 1 1 1 1 1 1 1	127						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 0 0 0 0 0 0 0	128						
0 1 0 0 0 0 0 0 1	129						
0 1 0 0 0 0 0 1 0	130						
0 1 0 0 0 0 0 1 1	131						
0 1 0 0 0 0 1 0 0	132						
0 1 0 0 0 0 1 0 1	133						
0 1 0 0 0 0 1 1 0	134						
0 1 0 0 0 0 1 1 1	135						
0 1 0 0 0 1 0 0 0	136						
0 1 0 0 0 1 0 0 1	137						
0 1 0 0 0 1 0 1 0	138						
0 1 0 0 0 1 0 1 1	139						
0 1 0 0 0 1 1 0 0	140						
0 1 0 0 0 1 1 0 1	141						
0 1 0 0 0 1 1 1 0	142						
0 1 0 0 0 1 1 1 1	143						
0 1 0 0 1 0 0 0 0	144						
0 1 0 0 1 0 0 0 1	145						
0 1 0 0 1 0 0 1 0	146						
0 1 0 0 1 0 0 1 1	147						
0 1 0 0 1 0 1 0 0	148						
0 1 0 0 1 0 1 0 1	149						
0 1 0 0 1 0 1 1 0	150						
0 1 0 0 1 0 1 1 1	151						
0 1 0 0 1 1 0 0 0	152						
0 1 0 0 1 1 0 0 1	153						
0 1 0 0 1 1 0 1 0	154						
0 1 0 0 1 1 0 1 1	155						
0 1 0 0 1 1 1 0 0	156						
0 1 0 0 1 1 1 0 1	157						
0 1 0 0 1 1 1 1 0	158						
0 1 0 0 1 1 1 1 1	159						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 0 1 0 0 0 0 0	160						
0 1 0 1 0 0 0 0 1	161						
0 1 0 1 0 0 0 1 0	162						
0 1 0 1 0 0 0 1 1	163						
0 1 0 1 0 0 1 0 0	164						
0 1 0 1 0 0 1 0 1	165						
0 1 0 1 0 0 1 1 0	166						
0 1 0 1 0 0 1 1 1	167						
0 1 0 1 0 1 0 0 0	168						
0 1 0 1 0 1 0 0 1	169						
0 1 0 1 0 1 0 1 0	170						
0 1 0 1 0 1 0 1 1	171						
0 1 0 1 0 1 1 0 0	172						
0 1 0 1 0 1 1 0 1	173						
0 1 0 1 0 1 1 1 0	174						
0 1 0 1 0 1 1 1 1	175						
0 1 0 1 1 0 0 0 0	176						
0 1 0 1 1 0 0 0 1	177						
0 1 0 1 1 0 0 1 0	178						
0 1 0 1 1 0 0 1 1	179						
0 1 0 1 1 0 1 0 0	180						
0 1 0 1 1 0 1 0 1	181						
0 1 0 1 1 0 1 1 0	182						
0 1 0 1 1 0 1 1 1	183						
0 1 0 1 1 1 0 0 0	184						
0 1 0 1 1 1 0 0 1	185						
0 1 0 1 1 1 0 1 0	186						
0 1 0 1 1 1 0 1 1	187						
0 1 0 1 1 1 1 0 0	188						
0 1 0 1 1 1 1 0 1	189						
0 1 0 1 1 1 1 1 0	190						
0 1 0 1 1 1 1 1 1	191						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 1 0 0 0 0 0 0	192						
0 1 1 0 0 0 0 0 1	193						
0 1 1 0 0 0 0 1 0	194						
0 1 1 0 0 0 0 1 1	195						
0 1 1 0 0 0 1 0 0	196						
0 1 1 0 0 0 1 0 1	197						
0 1 1 0 0 0 1 1 0	198						
0 1 1 0 0 0 1 1 1	199						
0 1 1 0 0 1 0 0 0	200						
0 1 1 0 0 1 0 0 1	201						
0 1 1 0 0 1 0 1 0	202						
0 1 1 0 0 1 0 1 1	203						
0 1 1 0 0 1 1 0 0	204						
0 1 1 0 0 1 1 0 1	205						
0 1 1 0 0 1 1 1 0	206						
0 1 1 0 0 1 1 1 1	207						
0 1 1 0 1 0 0 0 0	208						
0 1 1 0 1 0 0 0 1	209						
0 1 1 0 1 0 0 1 0	210						
0 1 1 0 1 0 0 1 1	211						
0 1 1 0 1 0 1 0 0	212						
0 1 1 0 1 0 1 0 1	213						
0 1 1 0 1 0 1 1 0	214						
0 1 1 0 1 0 1 1 1	215						
0 1 1 0 1 1 0 0 0	216						
0 1 1 0 1 1 0 0 1	217						
0 1 1 0 1 1 0 1 0	218						
0 1 1 0 1 1 0 1 1	219						
0 1 1 0 1 1 1 0 0	220						
0 1 1 0 1 1 1 0 1	221						
0 1 1 0 1 1 1 1 0	222						
0 1 1 0 1 1 1 1 1	223						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
0 1 1 1 0 0 0 0 0	224						
0 1 1 1 0 0 0 0 1	225						
0 1 1 1 0 0 0 1 0	226						
0 1 1 1 0 0 0 1 1	227						
0 1 1 1 0 0 1 0 0	228						
0 1 1 1 0 0 1 0 1	229						
0 1 1 1 0 0 1 1 0	230						
0 1 1 1 0 0 1 1 1	231						
0 1 1 1 0 1 0 0 0	232						
0 1 1 1 0 1 0 0 1	233						
0 1 1 1 0 1 0 1 0	234						
0 1 1 1 0 1 0 1 1	235						
0 1 1 1 0 1 1 0 0	236						
0 1 1 1 0 1 1 0 1	237						
0 1 1 1 0 1 1 1 0	238						
0 1 1 1 0 1 1 1 1	239						
0 1 1 1 1 0 0 0 0	240						
0 1 1 1 1 0 0 0 1	241						
0 1 1 1 1 0 0 1 0	242						
0 1 1 1 1 0 0 1 1	243						
0 1 1 1 1 0 1 0 0	244						
0 1 1 1 1 0 1 0 1	245						
0 1 1 1 1 0 1 1 0	246						
0 1 1 1 1 0 1 1 1	247						
0 1 1 1 1 1 0 0 0	248						
0 1 1 1 1 1 0 0 1	249						
0 1 1 1 1 1 0 1 0	250						
0 1 1 1 1 1 0 1 1	251						
0 1 1 1 1 1 1 0 0	252						
0 1 1 1 1 1 1 0 1	253						
0 1 1 1 1 1 1 1 0	254						
0 1 1 1 1 1 1 1 1	255						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 0 0 0 0 0 0 0 0	256						
1 0 0 0 0 0 0 0 1	257						
1 0 0 0 0 0 0 1 0	258						
1 0 0 0 0 0 0 1 1	259						
1 0 0 0 0 0 1 0 0	260						
1 0 0 0 0 0 1 0 1	261						
1 0 0 0 0 0 1 1 0	262						
1 0 0 0 0 0 1 1 1	263						
1 0 0 0 0 1 0 0 0	264						
1 0 0 0 0 1 0 0 1	265						
1 0 0 0 0 1 0 1 0	266						
1 0 0 0 0 1 0 1 1	267						
1 0 0 0 0 1 1 0 0	268						
1 0 0 0 0 1 1 0 1	269						
1 0 0 0 0 1 1 1 0	270						
1 0 0 0 0 1 1 1 1	271						
1 0 0 0 1 0 0 0 0	272						
1 0 0 0 1 0 0 0 1	273						
1 0 0 0 1 0 0 1 0	274						
1 0 0 0 1 0 0 1 1	275						
1 0 0 0 1 0 1 0 0	276						
1 0 0 0 1 0 1 0 1	277						
1 0 0 0 1 0 1 1 0	278						
1 0 0 0 1 0 1 1 1	279						
1 0 0 0 1 1 0 0 0	280						
1 0 0 0 1 1 0 0 1	281						
1 0 0 0 1 1 0 1 0	282						
1 0 0 0 1 1 0 1 1	283						
1 0 0 0 1 1 1 0 0	284						
1 0 0 0 1 1 1 0 1	285						
1 0 0 0 1 1 1 1 0	286						
1 0 0 0 1 1 1 1 1	287						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 0 0 1 0 0 0 0 0	288						
1 0 0 1 0 0 0 0 1	289						
1 0 0 1 0 0 0 1 0	290						
1 0 0 1 0 0 0 1 1	291						
1 0 0 1 0 0 1 0 0	292						
1 0 0 1 0 0 1 0 1	293						
1 0 0 1 0 0 1 1 0	294						
1 0 0 1 0 0 1 1 1	295						
1 0 0 1 0 1 0 0 0	296						
1 0 0 1 0 1 0 0 1	297						
1 0 0 1 0 1 0 1 0	298						
1 0 0 1 0 1 0 1 1	299						
1 0 0 1 0 1 1 0 0	300						
1 0 0 1 0 1 1 0 1	301						
1 0 0 1 0 1 1 1 0	302						
1 0 0 1 0 1 1 1 1	303						
1 0 0 1 1 0 0 0 0	304						
1 0 0 1 1 0 0 0 1	305						
1 0 0 1 1 0 0 1 0	306						
1 0 0 1 1 0 0 1 1	307						
1 0 0 1 1 0 1 0 0	308						
1 0 0 1 1 0 1 0 1	309						
1 0 0 1 1 0 1 1 0	310						
1 0 0 1 1 0 1 1 1	311						
1 0 0 1 1 1 0 0 0	312						
1 0 0 1 1 1 0 0 1	313						
1 0 0 1 1 1 0 1 0	314						
1 0 0 1 1 1 0 1 1	315						
1 0 0 1 1 1 1 0 0	316						
1 0 0 1 1 1 1 0 1	317						
1 0 0 1 1 1 1 1 0	318						
1 0 0 1 1 1 1 1 1	319						

ADDRESS A9 A8 A7 A6 A5 A4 A3 A2 A1	DECIMAL ADDRESS	OUTPUT DATA 05	04	03	02	01	USER'S CHAR.
1 0 1 0 0 0 0 0 0	320						
1 0 1 0 0 0 0 0 1	321						
1 0 1 0 0 0 0 1 0	322						
1 0 1 0 0 0 0 1 1	323						
1 0 1 0 0 0 1 0 0	324						
1 0 1 0 0 0 1 0 1	325						
1 0 1 0 0 0 1 1 0	326						
1 0 1 0 0 0 1 1 1	327						
1 0 1 0 0 1 0 0 0	328						
1 0 1 0 0 1 0 0 1	329						
1 0 1 0 0 1 0 1 0	330						
1 0 1 0 0 1 0 1 1	331						
1 0 1 0 0 1 1 0 0	332						
1 0 1 0 0 1 1 0 1	333						
1 0 1 0 0 1 1 1 0	334						
1 0 1 0 0 1 1 1 1	335						
1 0 1 0 1 0 0 0 0	336						
1 0 1 0 1 0 0 0 1	337						
1 0 1 0 1 0 0 1 0	338						
1 0 1 0 1 0 0 1 1	339						
1 0 1 0 1 0 1 0 0	340						
1 0 1 0 1 0 1 0 1	341						
1 0 1 0 1 0 1 1 0	342						
1 0 1 0 1 0 1 1 1	343						
1 0 1 0 1 1 0 0 0	344						
1 0 1 0 1 1 0 0 1	345						
1 0 1 0 1 1 0 1 0	346						
1 0 1 0 1 1 0 1 1	347						
1 0 1 0 1 1 1 0 0	348						
1 0 1 0 1 1 1 0 1	349						
1 0 1 0 1 1 1 1 0	350						
1 0 1 0 1 1 1 1 1	351						

ADDRESS A9 A8 A7 A6 A5 A4 A3 A2 A1	DECIMAL ADDRESS	OUTPUT DATA 05	04	03	02	01	USER'S CHAR.
1 0 1 1 0 0 0 0 0	352						
1 0 1 1 0 0 0 0 1	353						
1 0 1 1 0 0 0 1 0	354						
1 0 1 1 0 0 0 1 1	355						
1 0 1 1 0 0 1 0 0	356						
1 0 1 1 0 0 1 0 1	357						
1 0 1 1 0 0 1 1 0	358						
1 0 1 1 0 0 1 1 1	359						
1 0 1 1 0 1 0 0 0	360						
1 0 1 1 0 1 0 0 1	361						
1 0 1 1 0 1 0 1 0	362						
1 0 1 1 0 1 0 1 1	363						
1 0 1 1 0 1 1 0 0	364						
1 0 1 1 0 1 1 0 1	365						
1 0 1 1 0 1 1 1 0	366						
1 0 1 1 0 1 1 1 1	367						
1 0 1 1 1 0 0 0 0	368						
1 0 1 1 1 0 0 0 1	369						
1 0 1 1 1 0 0 1 0	370						
1 0 1 1 1 0 0 1 1	371						
1 0 1 1 1 0 1 0 0	372						
1 0 1 1 1 0 1 0 1	373						
1 0 1 1 1 0 1 1 0	374						
1 0 1 1 1 0 1 1 1	375						
1 0 1 1 1 1 0 0 0	376						
1 0 1 1 1 1 0 0 1	377						
1 0 1 1 1 1 0 1 0	378						
1 0 1 1 1 1 0 1 1	379						
1 0 1 1 1 1 1 0 0	380						
1 0 1 1 1 1 1 0 1	381						
1 0 1 1 1 1 1 1 0	382						
1 0 1 1 1 1 1 1 1	383						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 0 0 0 0 0 0 0	384						
1 1 0 0 0 0 0 0 1	385						
1 1 0 0 0 0 0 1 0	386						
1 1 0 0 0 0 0 1 1	387						
1 1 0 0 0 0 1 0 0	388						
1 1 0 0 0 0 1 0 1	389						
1 1 0 0 0 0 1 1 0	390						
1 1 0 0 0 0 1 1 1	391						
1 1 0 0 0 1 0 0 0	392						
1 1 0 0 0 1 0 0 1	393						
1 1 0 0 0 1 0 1 0	394						
1 1 0 0 0 1 0 1 1	395						
1 1 0 0 0 1 1 0 0	396						
1 1 0 0 0 1 1 0 1	397						
1 1 0 0 0 1 1 1 0	398						
1 1 0 0 0 1 1 1 1	399						
1 1 0 0 1 0 0 0 0	400						
1 1 0 0 1 0 0 0 1	401						
1 1 0 0 1 0 0 1 0	402						
1 1 0 0 1 0 0 1 1	403						
1 1 0 0 1 0 1 0 0	404						
1 1 0 0 1 0 1 0 1	405						
1 1 0 0 1 0 1 1 0	406						
1 1 0 0 1 0 1 1 1	407						
1 1 0 0 1 1 0 0 0	408						
1 1 0 0 1 1 0 0 1	409						
1 1 0 0 1 1 0 1 0	410						
1 1 0 0 1 1 0 1 1	411						
1 1 0 0 1 1 1 0 0	412						
1 1 0 0 1 1 1 0 1	413						
1 1 0 0 1 1 1 1 0	414						
1 1 0 0 1 1 1 1 1	415						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 0 1 0 0 0 0 0	416						
1 1 0 1 0 0 0 0 1	417						
1 1 0 1 0 0 0 1 0	418						
1 1 0 1 0 0 0 1 1	419						
1 1 0 1 0 0 1 0 0	420						
1 1 0 1 0 0 1 0 1	421						
1 1 0 1 0 0 1 1 0	422						
1 1 0 1 0 0 1 1 1	423						
1 1 0 1 0 1 0 0 0	424						
1 1 0 1 0 1 0 0 1	425						
1 1 0 1 0 1 0 1 0	426						
1 1 0 1 0 1 0 1 1	427						
1 1 0 1 0 1 1 0 0	428						
1 1 0 1 0 1 1 0 1	429						
1 1 0 1 0 1 1 1 0	430						
1 1 0 1 0 1 1 1 1	431						
1 1 0 1 1 0 0 0 0	432						
1 1 0 1 1 0 0 0 1	433						
1 1 0 1 1 0 0 1 0	434						
1 1 0 1 1 0 0 1 1	435						
1 1 0 1 1 0 1 0 0	436						
1 1 0 1 1 0 1 0 1	437						
1 1 0 1 1 0 1 1 0	438						
1 1 0 1 1 0 1 1 1	439						
1 1 0 1 1 1 0 0 0	440						
1 1 0 1 1 1 0 0 1	441						
1 1 0 1 1 1 0 1 0	442						
1 1 0 1 1 1 0 1 1	443						
1 1 0 1 1 1 1 0 0	444						
1 1 0 1 1 1 1 0 1	445						
1 1 0 1 1 1 1 1 0	446						
1 1 0 1 1 1 1 1 1	447						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 1 0 0 0 0 0 0	448						
1 1 1 0 0 0 0 0 1	449						
1 1 1 0 0 0 0 1 0	450						
1 1 1 0 0 0 0 1 1	451						
1 1 1 0 0 0 1 0 0	452						
1 1 1 0 0 0 1 0 1	453						
1 1 1 0 0 0 1 1 0	454						
1 1 1 0 0 0 1 1 1	455						
1 1 1 0 0 1 0 0 0	456						
1 1 1 0 0 1 0 0 1	457						
1 1 1 0 0 1 0 1 0	458						
1 1 1 0 0 1 0 1 1	459						
1 1 1 0 0 1 1 0 0	460						
1 1 1 0 0 1 1 0 1	461						
1 1 1 0 0 1 1 1 0	462						
1 1 1 0 0 1 1 1 1	463						
1 1 1 0 1 0 0 0 0	464						
1 1 1 0 1 0 0 0 1	465						
1 1 1 0 1 0 0 1 0	466						
1 1 1 0 1 0 0 1 1	467						
1 1 1 0 1 0 1 0 0	468						
1 1 1 0 1 0 1 0 1	469						
1 1 1 0 1 0 1 1 0	470						
1 1 1 0 1 0 1 1 1	471						
1 1 1 0 1 1 0 0 0	472						
1 1 1 0 1 1 0 0 1	473						
1 1 1 0 1 1 0 1 0	474						
1 1 1 0 1 1 0 1 1	475						
1 1 1 0 1 1 1 0 0	476						
1 1 1 0 1 1 1 0 1	477						
1 1 1 0 1 1 1 1 0	478						
1 1 1 0 1 1 1 1 1	479						

ADDRESS	DECIMAL ADDRESS	OUTPUT DATA					USER'S CHAR.
A9 A8 A7 A6 A5 A4 A3 A2 A1		05	04	03	02	01	
1 1 1 1 0 0 0 0 0	480						
1 1 1 1 0 0 0 0 1	481						
1 1 1 1 0 0 0 1 0	482						
1 1 1 1 0 0 0 1 1	483						
1 1 1 1 0 0 1 0 0	484						
1 1 1 1 0 0 1 0 1	485						
1 1 1 1 0 0 1 1 0	486						
1 1 1 1 0 0 1 1 1	487						
1 1 1 1 0 1 0 0 0	488						
1 1 1 1 0 1 0 0 1	489						
1 1 1 1 0 1 0 1 0	490						
1 1 1 1 0 1 0 1 1	491						
1 1 1 1 0 1 1 0 0	492						
1 1 1 1 0 1 1 0 1	493						
1 1 1 1 0 1 1 1 0	494						
1 1 1 1 0 1 1 1 1	495						
1 1 1 1 1 0 0 0 0	496						
1 1 1 1 1 0 0 0 1	497						
1 1 1 1 1 0 0 1 0	498						
1 1 1 1 1 0 0 1 1	499						
1 1 1 1 1 0 1 0 0	500						
1 1 1 1 1 0 1 0 1	501						
1 1 1 1 1 0 1 1 0	502						
1 1 1 1 1 0 1 1 1	503						
1 1 1 1 1 1 0 0 0	504						
1 1 1 1 1 1 0 0 1	505						
1 1 1 1 1 1 0 1 0	506						
1 1 1 1 1 1 0 1 1	507						
1 1 1 1 1 1 1 0 0	508						
1 1 1 1 1 1 1 0 1	509						
1 1 1 1 1 1 1 1 0	510						
1 1 1 1 1 1 1 1 1	511						

signetics

64X6X8 STATIC CHARACTER GENERATOR | 2516

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2516 is a 3072-bit Static ROM organized as 64x6x8. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State outputs for direct, low cost interfacing with TTL, DTL and 2500 Series MOS.

FEATURES

- COLUMN OUTPUT (VERTICAL SCAN)
- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT
- 2516/CM 2150 ASCII FONT STANDARD (5 x 7)
- 24-PIN DIP PACKAGE
- P-MOS SILICON GATE TECHNOLOGY

APPLICATIONS

VERTICAL SCAN CRT DISPLAYS
PRINTER CHARACTER GENERATORS
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

BIPOLAR COMPATIBILITY

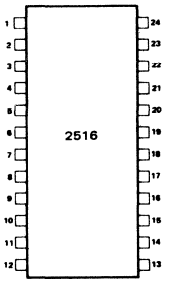
All inputs of the 2516 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA, sufficient to drive one standard TTL load.

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report."

PIN CONFIGURATION (Top View)

N/I PACKAGES



1. Chip Enable
2. NC
3. Output 8
4. Output 7
5. Output 6
6. Output 5
7. Output 4
8. Output 3
9. Output 2
10. Output 1
11. Ground
12. V_{DD}
13. NC
14. Address 1
15. Address 2
16. Address 3
17. Address 4
18. Address 5
19. Address 6
20. Address 7
21. Address 8
22. Address 9
23. V_{GG}
24. V_{CC}

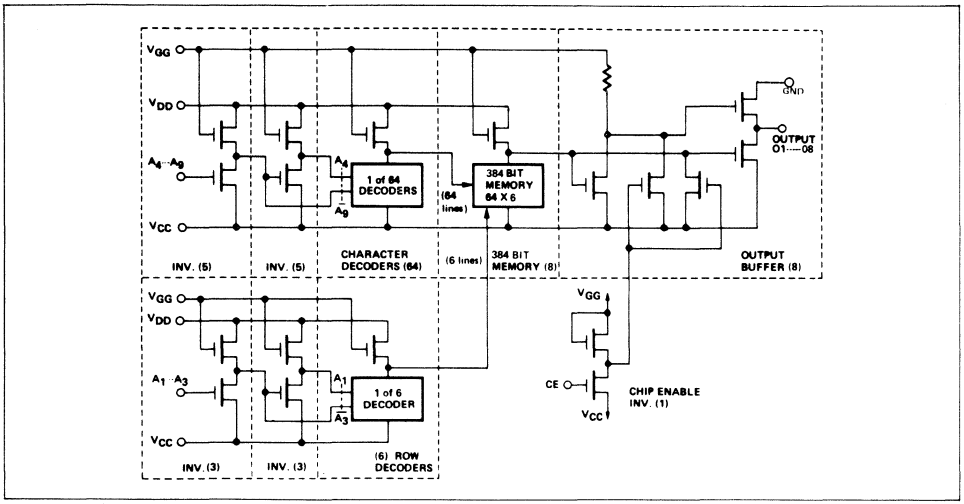
AC CHARACTERISTICS

T_A =0°C to +70°C; V_{CC} = 5V ±5% ±5%; V_{DD} = −5V ±5%; V_{GG} = −12V ±5%; unless otherwise noted.

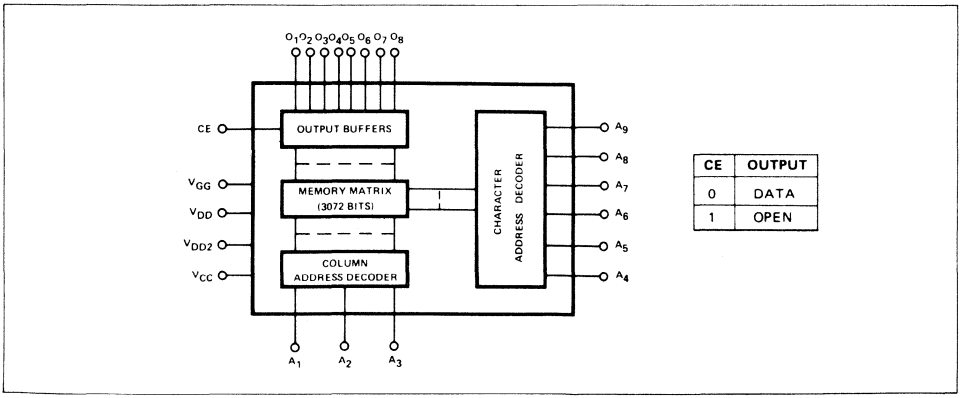
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		+0.5	V(8)	I_{OL} = 1.6mA
V_{OH}	Output Logic "One"	+3.8			V(8)	I_{OH} = 100μA
t_{CA}	Character Access Time		500	600	ns	See AC Test Setup*
t_{CA}	Column Access Time (A_1 - A_3)		400	500	ns	See AC Test Setup*
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{IH} = V_{CC}, 25mV p-p

*T_A=0°C to +70°C

CIRCUIT SCHEMATIC



BLOCK DIAGRAM



CE	OUTPUT
0	DATA
1	OPEN

PART IDENTIFICATION TABLE

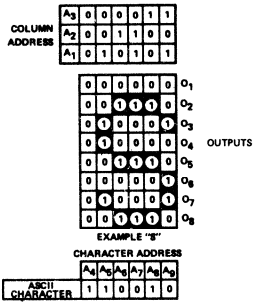
PART	ORGANIZATION	PROGRAMMING
2516N/I CM 2150	64 x 6 x 8	ASCII Font
2516N/I CMXXXX	64 x 6 x 8	Custom

N Package = 24 Pin Silicone DIP
I Package = 24 Pin Ceramic DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @ 70°C	730 mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

CHARACTER FORMAT



NOTE:
Undefined (column) addresses result in "1" level (high) outputs.

NOTES

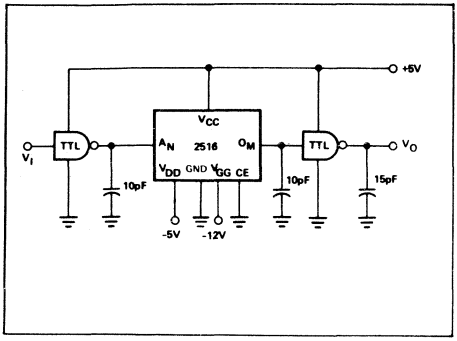
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.

DC CHARACTERISTICS

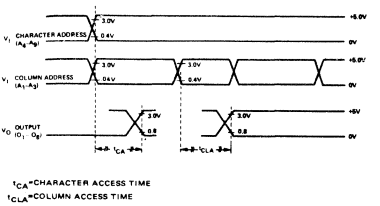
T_A = 0°C to +70°C; V_{CC} = +5 V ±5% ; V_{DD} = -5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted. (Notes 4, 5, 6 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C
I_{DD}	V_{DD} Power Supply Current		14	21	mA	V_{CE} = V_{CC} Outputs Open
I_{GG}	V_{GG} Power Supply Current		8	12	mA	Outputs Open
V_{IL}	Input Logic "0"	-5		+0.6	V	Note 8
V_{IH}	Input Logic "1"	+3.4		5.3	V	Note 8

AC TEST SETUP



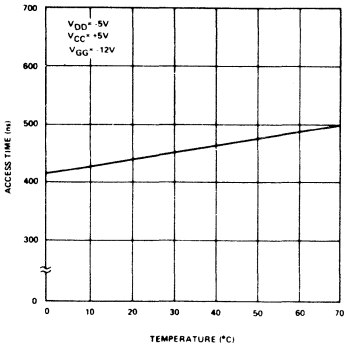
TIMING DIAGRAM



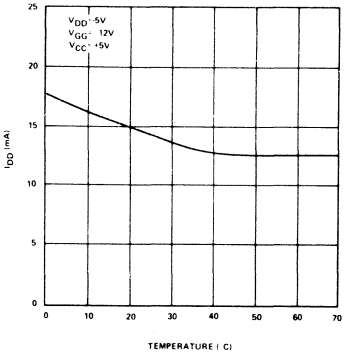
t_{CA}=CHARACTER ACCESS TIME
t_{CLA}=COLUMN ACCESS TIME

TYPICAL CHARACTERISTIC CURVES

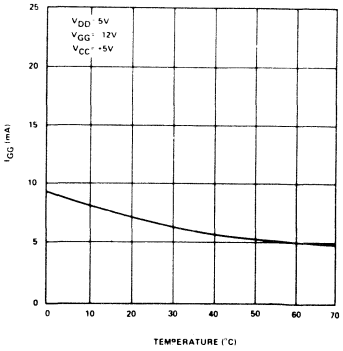
TYPICAL ACCESS TIME VERSUS TEMPERATURE



V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



APPLICATIONS DATA:

OUTPUT INTERFACING NOTES

The tri-state outputs on this device exhibit three states:

"1" – low impedance to +5V
"0" – low impedance to -5V
OFF – high impedance >10 megohm

The "off" state is controlled by the chip enable control input.

CUSTOM ROM ORGANIZATIONS

The 2516 is a static ROM with a total 64 x 6 x 8 bit capacity. This allows a standard 5 x 7 font to be encoded in the ROM, e.g., the 2516/CM2150 ASCII font standard product. A custom coding configuration may make use of the full 6x8 dot matrix if desired.

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 6 dots horizontally and 8 dots vertically. A three bit-binary address code (A_1 through A_3) selects 1 of 6 columns. Eight outputs display a complete column of the character matrix.

STANDARD PATTERN

A standard ASCII Character Font is available for the 2516. This device (2516N / CM2150) may be used for ASCII character generation or for device evaluation.

CUSTOM DEVICES

For unique custom memory patterns, the following formats should be used to transmit coding instructions. The nomenclature for each custom device will consist of the basic product type followed by a unique "CM" number assigned by Signetics. For example, "2516N/CM2151",

- **Programming with punched cards.**
  For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.

- **Programming with written truth table.**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

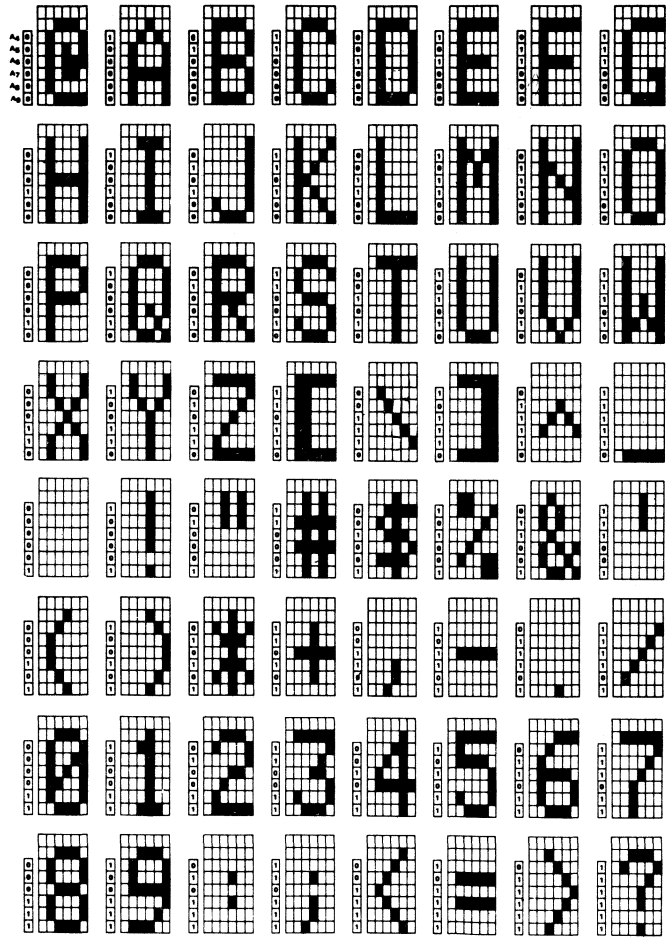
LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. +3.6V minimum). Similarly, a "1" address input level is interpreted as +3.2V minimum.

Undefined addresses result in "1" level outputs.

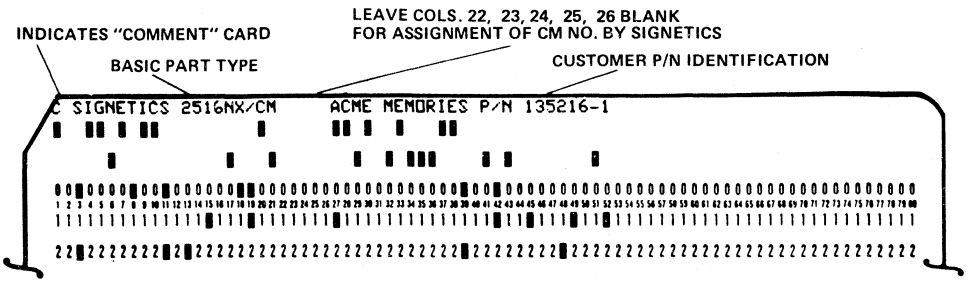
ASCII CHARACTER FONT

2516N/CM2150

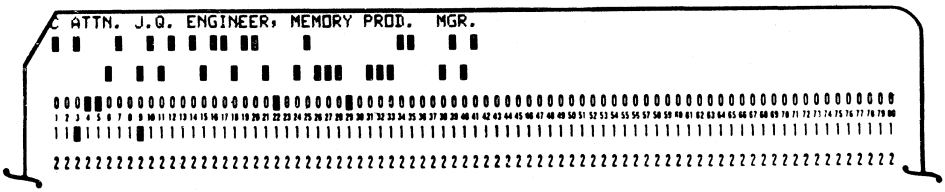


NOTE: Excess addresses yield logic "1" outputs.

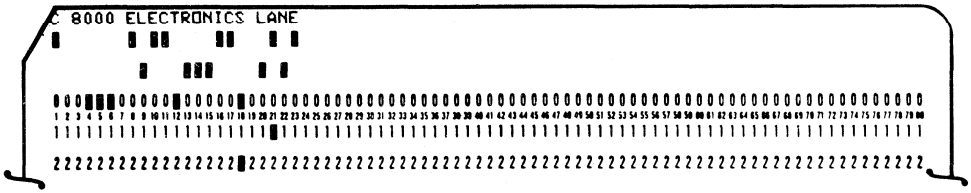
IDENTIFICATION CARDS



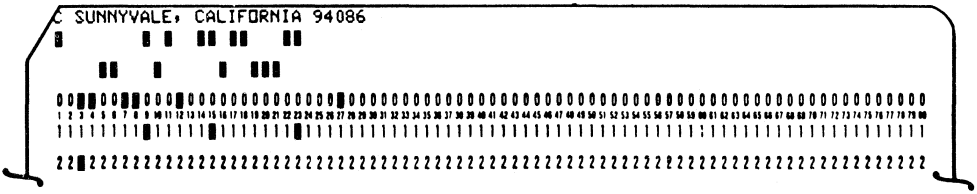
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS
COMPUTER GENERATED TRUTH TABLE



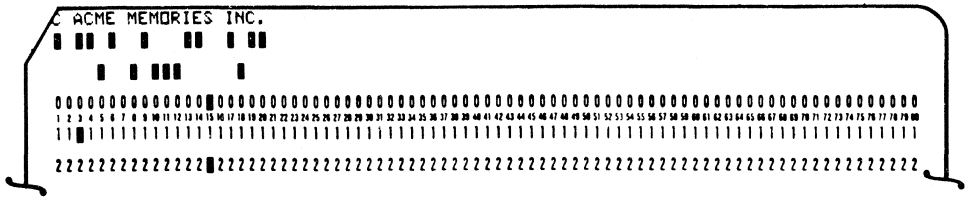
STREET ADDRESS



CITY STATE ZIP



COMPANY NAME

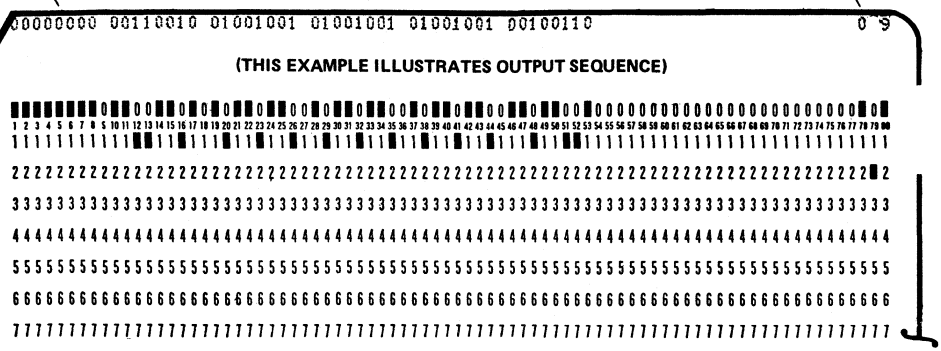


SIGNETICS 64 X 6 X 8 STATIC CHARACTER GENERATOR ■ 2516

DATA CARDS

OUTPUTS O_R THROUGH O_1 RESPECTIVELY

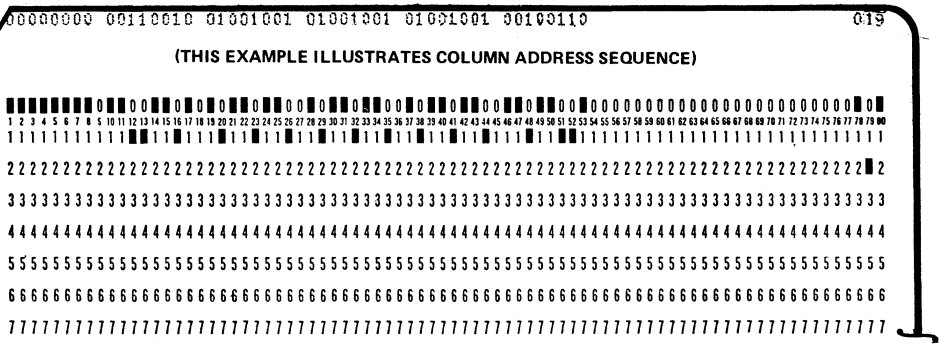
DECIMAL CHARACTER ADDRESS
(DATA CARD NUMBER 001 THRU 064)



(THIS EXAMPLE ILLUSTRATES OUTPUT SEQUENCE)

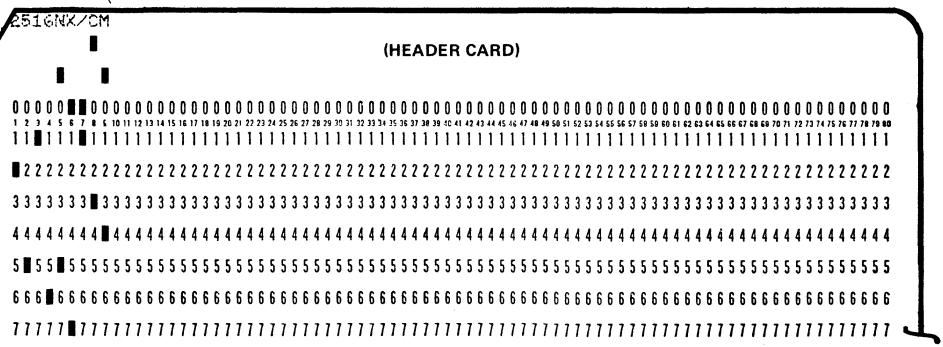
COLUMN ADDRESS(A_3,A_2,A_1)

000 001 010 011 100 101



(THIS EXAMPLE ILLUSTRATES COLUMN ADDRESS SEQUENCE)

BASIC DEVICE TYPE
LEAVE COLS. 10, 11, 12, 13 BLANK FOR ASSIGNMENT OF CM NO. BY SIGNETICS



(HEADER CARD)

NOTE
"Character" number is in columns 78, 79, and 80.

Character Number						001
Column Binary Address	Column Decimal Address					
	000	001	002	003	004	005
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						002
Column Binary Address	Column Decimal Address					
	008	009	010	011	012	013
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						003
Column Binary Address	Column Decimal Address					
	016	017	018	019	020	021
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						004
Column Binary Address	Column Decimal Address					
	024	025	026	027	028	029
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						005
Column Binary Address	Column Decimal Address					
	032	033	034	035	036	037
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						006
Column Binary Address	Column Decimal Address					
	040	041	042	043	044	045
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						007
Column Binary Address	Column Decimal Address					
	048	049	050	051	052	053
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						008
Column Binary Address	Column Decimal Address					
	056	057	058	059	060	061
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	009					
Column Binary Address	Column Decimal Address					
	064	065	066	067	068	069
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	010					
Column Binary Address	Column Decimal Address					
	072	073	074	075	076	077
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	011					
Column Binary Address	Column Decimal Address					
	080	081	082	083	084	085
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	012					
Column Binary Address	Column Decimal Address					
	088	089	090	091	092	093
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	013					
Column Binary Address	Column Decimal Address					
	096	097	098	099	100	101
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	014					
Column Binary Address	Column Decimal Address					
	104	105	106	107	108	109
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	015					
Column Binary Address	Column Decimal Address					
	112	113	114	115	116	117
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	016					
Column Binary Address	Column Decimal Address					
	120	121	122	123	124	125
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	017					
Column Binary Address	Column Decimal Address					
	128	129	130	131	132	133
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	018					
Column Binary Address	Column Decimal Address					
	136	137	138	139	140	141
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	019					
Column Binary Address	Column Decimal Address					
	144	145	146	147	148	149
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	020					
Column Binary Address	Column Decimal Address					
	152	153	154	155	156	157
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	021					
Column Binary Address	Column Decimal Address					
	160	161	162	163	164	165
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	022					
Column Binary Address	Column Decimal Address					
	168	169	170	171	172	173
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	023					
Column Binary Address	Column Decimal Address					
	176	177	178	179	180	181
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	024					
Column Binary Address	Column Decimal Address					
	184	185	186	187	188	189
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 025						
Column Binary Address	Column Decimal Address					
	192	193	194	195	196	197
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 026						
Column Binary Address	Column Decimal Address					
	200	201	202	203	204	205
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 027						
Column Binary Address	Column Decimal Address					
	208	209	210	211	212	213
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 028						
Column Binary Address	Column Decimal Address					
	216	217	218	219	220	221
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 029						
Column Binary Address	Column Decimal Address					
	224	225	226	227	228	229
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 030						
Column Binary Address	Column Decimal Address					
	232	233	234	235	236	237
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 031						
Column Binary Address	Column Decimal Address					
	240	241	242	243	244	245
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 032						
Column Binary Address	Column Decimal Address					
	248	249	250	251	252	253
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	0	0	0	0	0	0

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 033						
Column Binary Address	Column Decimal Address					
	256	257	258	259	260	261
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 034						
Column Binary Address	Column Decimal Address					
	264	265	266	267	268	269
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 035						
Column Binary Address	Column Decimal Address					
	272	273	274	275	276	277
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 036						
Column Binary Address	Column Decimal Address					
	280	281	282	283	284	285
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 037						
Column Binary Address	Column Decimal Address					
	288	289	290	291	292	293
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 038						
Column Binary Address	Column Decimal Address					
	296	297	298	299	300	301
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 039						
Column Binary Address	Column Decimal Address					
	304	305	306	307	308	309
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 040						
Column Binary Address	Column Decimal Address					
	312	313	314	315	316	317
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	041					
Column Binary Address	Column Decimal Address					
	320	321	322	323	324	325
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	042					
Column Binary Address	Column Decimal Address					
	328	329	330	331	332	333
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	043					
Column Binary Address	Column Decimal Address					
	336	337	338	339	340	341
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	044					
Column Binary Address	Column Decimal Address					
	344	345	346	347	348	349
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	045					
Column Binary Address	Column Decimal Address					
	352	353	354	355	356	357
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	046					
Column Binary Address	Column Decimal Address					
	360	361	362	363	364	365
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	047					
Column Binary Address	Column Decimal Address					
	368	369	370	371	372	373
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number	048					
Column Binary Address	Column Decimal Address					
	376	377	378	379	380	381
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	0	0	0	0	0	0
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						049
Column Binary Address	Column Decimal Address					
	384	385	386	387	388	389
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						050
Column Binary Address	Column Decimal Address					
	392	393	394	395	396	397
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						051
Column Binary Address	Column Decimal Address					
	400	401	402	403	404	405
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						052
Column Binary Address	Column Decimal Address					
	408	409	410	411	412	413
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						053
Column Binary Address	Column Decimal Address					
	416	417	418	419	420	421
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						054
Column Binary Address	Column Decimal Address					
	424	425	426	427	428	429
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						055
Column Binary Address	Column Decimal Address					
	432	433	434	435	436	437
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number						056
Column Binary Address	Column Decimal Address					
	440	441	442	443	444	445
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	0	0	0	0	0	0
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 057						
Column Binary Address	Column Decimal Address					
	448	449	450	451	452	453
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 058						
Column Binary Address	Column Decimal Address					
	456	457	458	459	460	461
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 059						
Column Binary Address	Column Decimal Address					
	464	465	466	467	468	469
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 060						
Column Binary Address	Column Decimal Address					
	472	473	474	475	476	477
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	0	0	0	0	0	0
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 061						
Column Binary Address	Column Decimal Address					
	480	481	482	483	484	485
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 062						
Column Binary Address	Column Decimal Address					
	488	489	490	491	492	493
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	0	0	0	0	0	0
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 063						
Column Binary Address	Column Decimal Address					
	496	497	498	499	500	501
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	0	0	0	0	0	0
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

Character Number 064						
Column Binary Address	Column Decimal Address					
	504	505	506	507	508	509
A_1	0	1	0	1	0	1
A_2	0	0	1	1	0	0
A_3	0	0	0	0	1	1
A_4	1	1	1	1	1	1
A_5	1	1	1	1	1	1
A_6	1	1	1	1	1	1
A_7	1	1	1	1	1	1
A_8	1	1	1	1	1	1
A_9	1	1	1	1	1	1

Output	Output Codes					
O_1						
O_2						
O_3						
O_4						
O_5						
O_5						
O_7						
O_8						

signetics

64 x 9 x 9 ROM STATIC CHARACTER GENERATOR | 2526

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2526 is a high speed 5,184-bit Static Read-Only Memory. It may be organized as 64x9x9 for use as a character generator, or as a 512x9 ROM for general purpose use. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. OUTPUT ENABLE controls the nine output devices without affecting address circuitry.

FEATURES

- **64x9x9 ORGANIZATION**
- **512x9 ORGANIZATION**
- **625ns TYPICAL ACCESS TIME**
- **STATIC OPERATION**
- **OUTPUT LATCHES**
- **TTL/DTL COMPATIBLE INPUTS**
- **TTL/DTL COMPATIBLE TRI-STATE OUTPUTS**
- **V_{CC} = +5V, V_{GG} = −12V**
- **24-PIN SILICONE DIP**
- **P-MOS SILICON GATE TECHNOLOGY**

APPLICATIONS

VERTICAL OR RASTER SCAN DISPLAYS (7x9 MATRIX)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION
PROGRAM STORAGE

BIPOLAR COMPATIBILITY

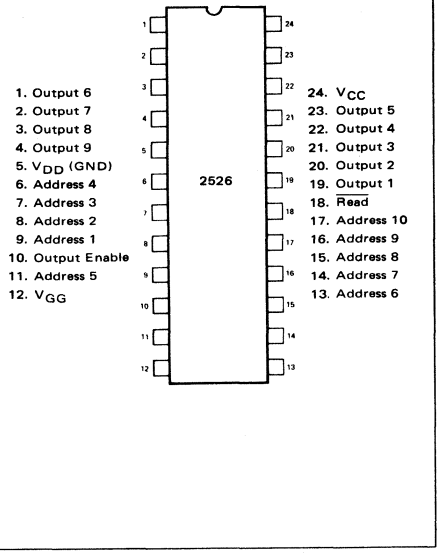
All inputs of the 2526 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA to drive one standard TTL load.

STANDARD CODES

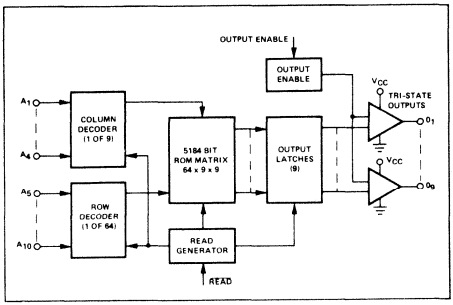
The 2526 is available with ASCII-addressed characters using a 7x9 dot matrix. The two remaining locations in the 9x9 matrix are used for BCDIC-to-ASCII and BAUDOT-to-ASCII code conversions. The 2526/CM3940 is organized for raster scan and the 2526/CM3400 is for vertical scan.

PIN CONFIGURATION (Top View)

N/I PACKAGES



BLOCK DIAGRAM



PART IDENTIFICATION

PART	OP. TEMP. RANGE	PACKAGE
2526N	0-70°C	24-Pin Silicone DIP
2526I	0-70°C	24-Pin Ceramic DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70°C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%; V_{GG} = −12V ±5%; unless otherwise noted. (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		30	45	mA	(8)
I_{GG}	V_{GG} Power Supply Current		30	45	mA	(8)
V_{IL}	Input Logic "0"	-5		+0.6	V	(13)
V_{IH}	Input Logic "1"	+3.4		5.3	V	(13)

AC CHARACTERISTICS

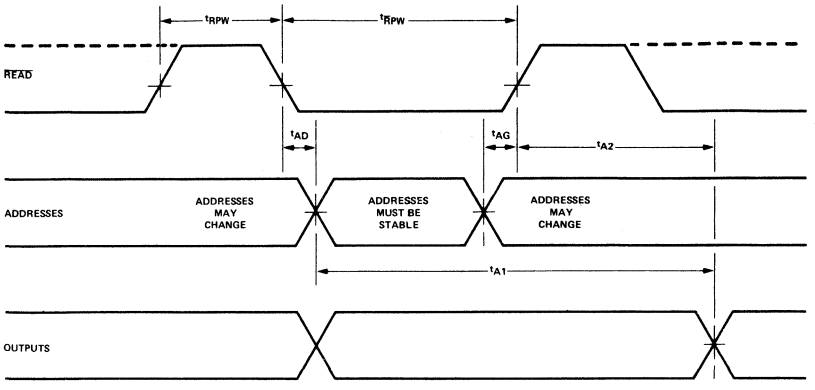
T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{GG} = −12V ±5%; unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "zero"			+.5	V	I_{OL} = 1.6mA
V_{OH}	Output Logic "one"	+3.8			V	I_{OH} = 100μA
t_{RPW}[11]	Read Pulse Width	250	200		ns	
$t_{\overline{RPW}}$[10]	$\overline{\text{Read}}$ Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (12)			50	ns	
t_{AG}	Address-Read Pulse Gap (12)			50	ns	
t_{A1}	Address to Output Delay		625	700	ns	(9)
t_{A2}	End of $\overline{\text{Read}}$ Pulse to Output Delay		200	250		(9)
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz,
t_{OE}	Output Enable to Output Delay		100	250	ns	V_{AC} = 25mV p-p V_{IN} = V_{CC}

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs Open, t_{RPW} = 250ns, $t_{\overline{RPW}}$ = 500ns.
9. t_A = 0°C to +70°C
10. During t_{RPW1} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
11. During $t_{\overline{RPW1}}$ addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{READ}}$ pulse. After t_{A2}, data appears at the output terminals.
12. Addresses must be stable within 50ns after the $\overline{\text{READ}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{READ}}$ line goes high.
13. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.

TIMING DIAGRAM



NOTE: All Times Measured from 50% Points.

$t_r = t_f = 10$ ns or less.

APPLICATION INFORMATION

The 2526 is organized to provide 64 character locations with each character described by a 9x9 matrix of bits. The six address inputs A5 through A10 are decoded directly to provide a 1-of-64 character selection. The four address inputs A1 through A4 are decoded to provide a 1-of-9 selection of scans within each character. Since four address lines can generate 16 scan selections instead of only 9, there are seven excess codes. The 1-of-9 scan decoder forces the excess input codes to generate all logic "0s" at the output latches.

The 9x9 dot configuration for each character allows the 2526 to be used as a 7x9 character generator with either vertical or horizontal scanning techniques. In the horizontal case, as each slice through the character is extracted from the ROM, the two extra bits may be ignored and the seven remaining bits used to control the dot formations. In the vertical case, each slice through the character provides the full nine bits needed to control the dots. Two complete scans are not used for dots and may be ignored or may be used for code translations.

For use as a 512x9 ROM, simply tie address A4 to a logical zero thus eliminating the excess input addresses. The other nine address lines can then be used to address 512 contiguous locations in the memory.

COLUMN DECODING

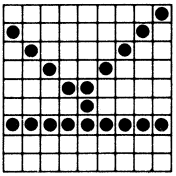
LOGIC 0 < 0.8 VOLTS

LOGIC 1 > 3.2 VOLTS

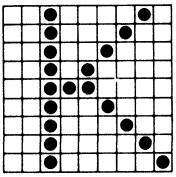
INPUT CODES

A4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1

EXCESS ADDRESSES



9 X 9 MATRIX HORIZONTAL SCAN



9 X 9 MATRIX VERTICAL SCAN

STANDARD CHARACTER FONT

CM 3400

ASCII SET, VERTICAL SCAN 7X9 WITH CODE CONVERSION

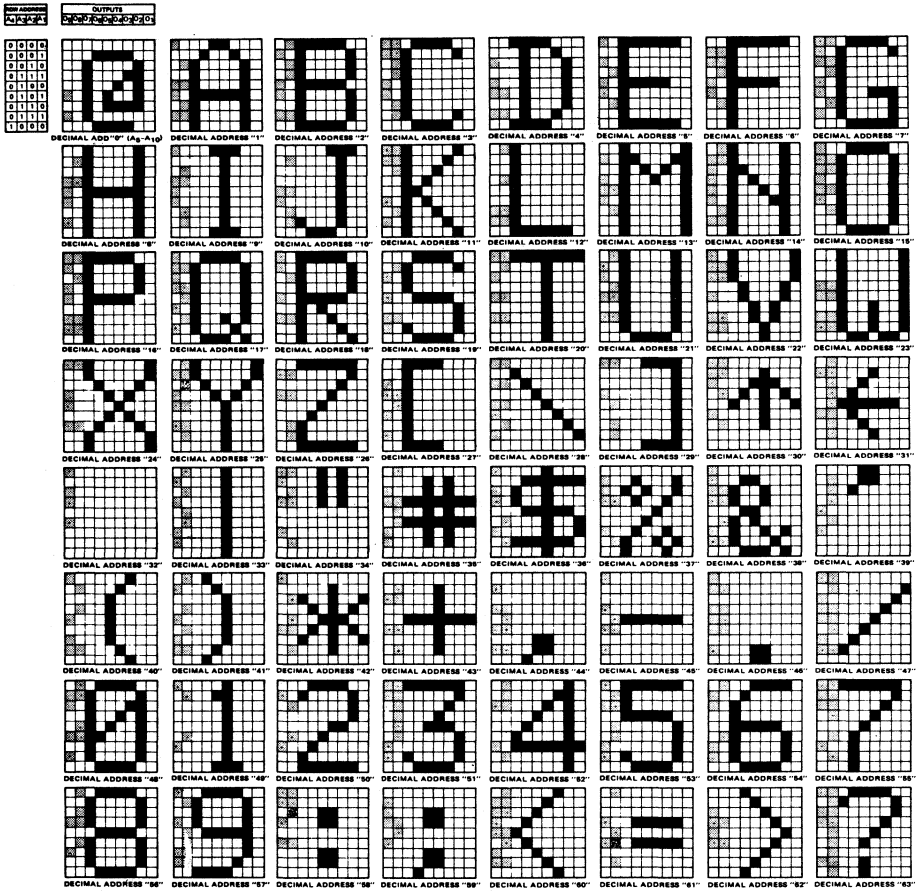
NOTES

1. BCDIC to ASCII in leftmost column, Baudot to ASCII in next column to right.
2. Undefined addresses result in all outputs going low (TTL "0").
3. Black squares in character font are high (TTL "1").

STANDARD CHARACTER FONT

CM 3941

ASCII SET, RASTER SCAN 7X9 WITH CODE CONVERSION



NOTES

1. BCDIC to ASCII in leftmost column, Baudot to ASCII in next column to right.
2. Undefined addresses result in all outputs going low (TTL "0").
3. Black squares in character font are high (TTL "1").

2526 CUSTOM CODING INFORMATION

PUNCHED CARD INPUT

Comment/I.D. Cards:

Card No.	Column	Information
1	1	"C"
	2	Blank
	3-17	"SIGNETICS 2526N/CM"
	18-26	Blank
	27-71	Customer I'D' (Company, Project, Part No., etc.)
	72	Blank
	73-80	Date
2	1	"C"
	2	Blank
	3-80	Person responsible for reviewing Signetics truth table.
3	1	"C"
	2	Blank
	3-80	Customer Street Address
4	1	"C"
	2	Blank
	3-80	Customer City, State, Zip.
5	1	"C"
	2	Blank
	3-80	Name

Data Cards

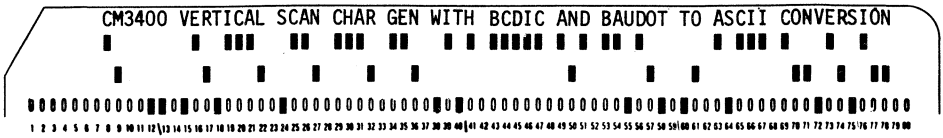
Card No.	Column	Information
1	1-9	Binary outputs of rows 9 through 1, (MSB at 9), first column, first character, (first character is "000"). Logic "1" is high output (3.2V, min.).
	10	Blank
	11-19	Binary outputs of second column, first character.
	20	Blank
	21-29	Third column

Data Cards (Continued)

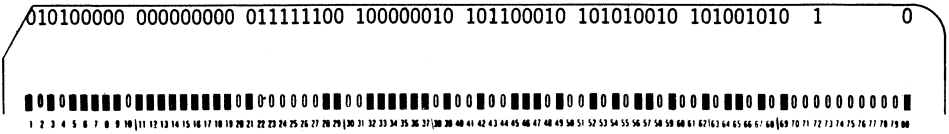
Card No.	Column	Information
1 (Cont'd)	30	Blank
	31-39	Fourth column
	40	Blank
	41-49	Fifth column
	50	Blank
	51-59	Sixth column
	60	Blank
	61-69	Seventh column
	70-71	Blank
	72	Data card number of first character, ("1").
	73	Blank
	74-76	Anything – customer option.
	77	Blank
	78-80	Decimal character number, ("000")
2	1-9	Eighth column
	10	Blank
	11-19	Ninth column
	20-70	Anything – customer option.
	71	Blank
	72	Data card number of first character, ("2").
	73	Blank
	74-76	Customer option
	77	Blank
	78-80	Decimal character number, ("000").
3	1-9 (Etc., as Card 1)	First column, second character, rows 9 through 1 (MSB at 9). Second character is "001".
4	(Etc., as Card 2)	
128	78-80	Decimal character number, ("063").

EXAMPLES:

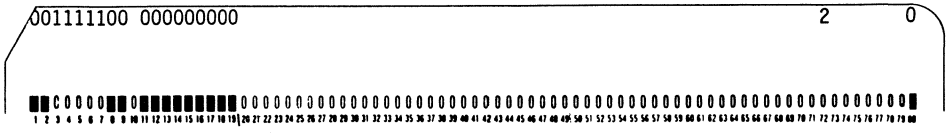
I.D. Card



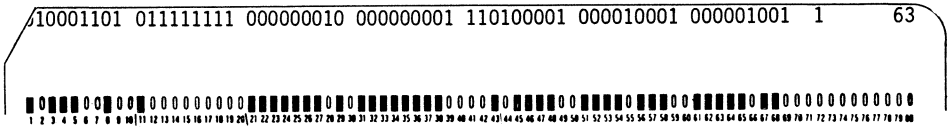
First Data Card – First Character



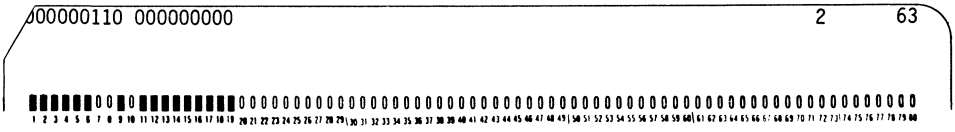
Second Data Card – First Character



First Data Card – Last Character



Second Data Card – Last Character



TRUTH TABLE INPUT: A truth table may be submitted at a greater non-recurring cost to the customer. A format similar to the one shown below is satisfactory.

ADDRESS										DECIMAL ADDRESS	OUTPUT DATA									CHARACTER
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1		O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	
0	0	0	0	0	0	0	0	0	0	000										↑ FIRST CHARACTER ↓
0	0	0	0	0	0	0	0	0	1	001										
0	0	0	0	0	0	0	0	1	0	002										
0	0	0	0	0	0	0	0	1	1	003										
0	0	0	0	0	0	0	1	0	0	004										
0	0	0	0	0	0	0	1	0	1	005										
0	0	0	0	0	0	0	1	1	0	006										
0	0	0	0	0	0	0	1	1	1	007										
0	0	0	0	0	0	1	0	0	0	008										
0	0	0	0	0	1	0	0	0	0	016										↑ SECOND CHARACTER ↓
0	0	0	0	0	1	0	0	0	1	017										
										Etc.										

signetics HIGH SPEED 512x8 STATIC READ-ONLY MEMORY | 2530

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2530 is a high speed 4,096-bit Static Read-Only Memory available in a 512x8 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. Two-mask programmable OUTPUT ENABLES control the eight output devices without affecting address circuitry.

FEATURES

- **512x8 ORGANIZATION**
- **625ns TYPICAL ACCESS TIME**
- **STATIC OPERATION**
- **ADDRESS LATCHES**
- **PROGRAMMABLE OUTPUT ENABLES**
- **TTL/DTL COMPATIBLE INPUTS**
- **THREE-STATE OUTPUTS**
- **V_{CC} = +5V, V_{GG} = −12V**
- **24-PIN SILICONE DIP**
- **P-MOS SILICON GATE TECHNOLOGY**

APPLICATIONS

MICRO-PROGRAMMING
CODE-CONVERSION
PROGRAM STORAGE

TTL COMPATIBILITY

All inputs of the 2530 can be driven directly by standard bipolar integrated circuits, (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

STANDARD TRUTH TABLES

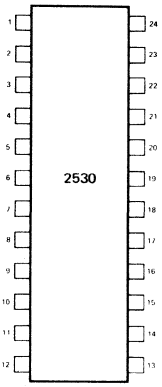
The 2530NX/CM3530 is an ASCII-EBCDIC and EBCDIC-ASCII code converter. Use this device for evaluation or for applications requiring this conversion.

PART IDENTIFICATION

PART	OP. TEMP. RANGE	PACKAGE
2530N	0-70°C	24-Pin Silicone DIP
2530I	0-70°C	24-Pin Ceramic DIP

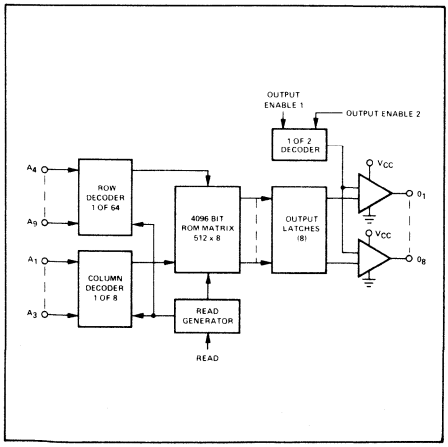
PIN CONFIGURATION (Top View)

N/I PACKAGES



1.	Output 6	24.	V_{CC}
2.	Output 7	23.	Output 5
3.	Output 8	22.	Output 4
4.	V_{DD} (Gnd)	21.	Output 3
5.	Address 1	20.	Output 2
6.	Address 2	19.	Output 1
7.	Address 3	18.	$\overline{\text{Read}}$
8.	Output Enable 1	17.	NC
9.	Output Enable 2	16.	Address 9
10.	Address 4	15.	Address 8
11.	Address 5	14.	Address 7
12.	V_{GG}	13.	Address 6

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70°C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A = 0° to +70°C, V_{CC} = +5V ± 5% ; V_{GG} = −12V ± 5%; unless otherwise noted. (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		30	45	mA	(8)
I_{GG}	V_{GG} Power Supply Current		30	45	mA	(8)
V_{IL}	Input Logic "0"	-5		+0.6	V	(13)
V_{IH}	Input Logic "1"	+3.4		5.3	V	(13)

AC CHARACTERISTICS

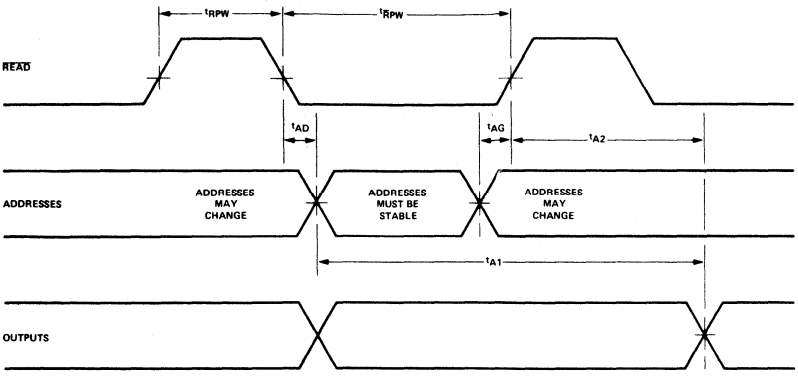
T_A = 0°C to 70°C; V_{CC} = 5V ± 5% ; V_{GG} = −12V ± 5%; unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "zero"			+0.5	V	I_{OL} = 1.6mA
V_{OH}	Output Logic "one"	+3.8			V	I_{OH} = 100μA
t_{RPW}[11]	Read Pulse Width	250	200		ns	
$t_{\overline{RPW}}$[10]	$\overline{\text{Read}}$ Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (12)			50	ns	
t_{AG}	Address-Read Pulse Gap (12)			50	ns	
t_{A1}	Address to Output Delay		625	700	ns	(9)
t_{A2}	End of $\overline{\text{Read}}$ Pulse to Output Delay		200	250		(9)
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}
t_{OE}	Output Enable to Output Delay		100	250	ns	

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs Open, t_{RPW} = 250ns, $t_{\overline{RPW}}$ = 500ns.
9. t_A = 0°C to +70°C
10. During $t_{\overline{RPW}1}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
11. During t_{RPW1} addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{READ}}$ pulse. After t_{A2}, data appears at the output terminals.
12. Addresses must be stable within 50ns after the $\overline{\text{READ}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{READ}}$ line goes high.
13. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.

TIMING DIAGRAM



Note: All times measured from 50% points for all input waveforms tr = tf<10nsec.

2530 CUSTOM CODING INFORMATION

TRUTH TABLE INPUT:

A truth table may be submitted at a greater non-recurring cost to the customer. A format similar to the one shown below is satisfactory.

INPUT ADDRESS									DECIMAL ADDRESS	OUTPUT							
A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0	0	0	0	0	0	0	0	0	000								
0	0	0	0	0	0	0	0	1	001								
1	1	1	1	1	1	1	1	0	510								
1	1	1	1	1	1	1	1	1	511								

Plus Output Enable 1 and 2 coding.

2530 CUSTOM CODING INFORMATION

PUNCHED CARD INPUT

Header Card

Card No.	Column	Information
1	1–5	"2530N" or "2530I"
	6–14	Blank
	15–19	"CODED"
	20	Blank
	21	Logic state of Output Enable #2, (CS2) - Most Significant Bit.
	22	Logic state of Output Enable #1.
	23	Blank
	24–71	Customer company name.
	72	Blank
	73–80	Date

I.D./Comment Cards:

Card No.	Column	Information
1	1	"C"
	2	Blank
	3–80	Person responsible for reviewing Signetics truth table and Company Name.
2	1	"C"
	2	Blank
	3–80	Customer Street Address
3	1	"C"
	2	Blank
	3–80	Customer City, State, Zip.

Data Cards:

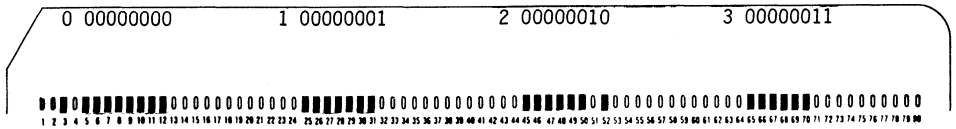
Card No.	Column	Information
1	1–3	Decimal address (blank, blank, 0.)
	4	Blank
	5–12	8-digit binary output (MSB-left)
	13–20	Blank
	21–33	Decimal address, (blank, blank, 1.)
	24	Blank
	25–32	8-Digit binary output (MSB-left)
	33–40	Blank
	41–43	Decimal address, (Blank, blank, 2.)
	44	Blank
	45–52	8-digit binary output (MSB-left)
	53–60	Blank
	61–63	Decimal address, (Blank, blank, 3.)
	64	Blank
	65–72	8-digit binary output (MSB-left)
	73–80	Blank
2 ⋮ 128		Same format as data card #1. Same format as data card #1.

NOTE: MSB = O_9

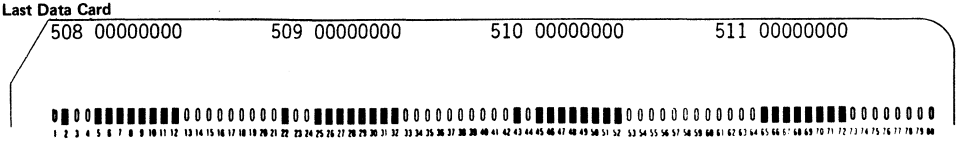
EXAMPLES:

Header Card

First Data Card



Last Data Card



signetics

8192- BIT STATIC READ-ONLY MEMORY 2580

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2580 is an 8,192-Bit Read-Only Memory available in a 2048x4 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A READ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. The outputs are enabled by a programmable four bit select code applied to four binary chip select terminals.

FEATURES

- 2048x4 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- OUTPUT LATCHES
- 1 OF 16 CHIP ENABLE DECODING
- TTL/DTL COMPATIBLE INPUTS AND OUTPUTS
- THREE-STATE OUTPUTS
- V_{CC} = +5V' V_{GG} = −12V, V_{DD} = 0V
- 24 PIN SILICONE DIP
- P-MOS SILICON GATE TECHNOLOGY

APPLICATIONS

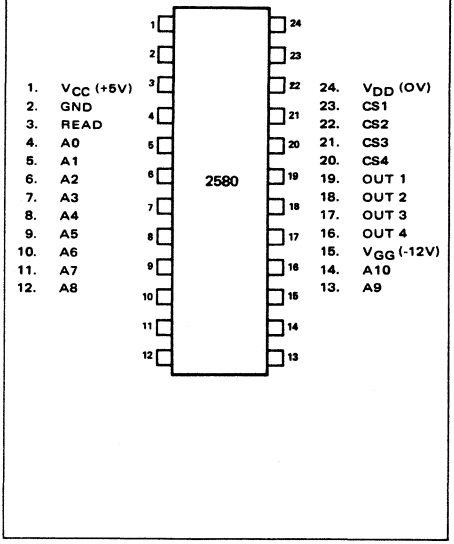
MICRO-PROGRAMMING
LOOK-UP TABLES
DATA STORAGE
CODE CONVERSION
RANDOM LOGIC SYNTHESIS
CHARACTER GENERATION
PROGRAM STORAGE

BIPOLAR COMPATIBILITY

All inputs of the 2580 can be driven directly by standard TTL level signals. The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N/I PACKAGES



PART IDENTIFICATION

PART NUMBER	OP. TEMP. RANGE	PACKAGE
2580N	0-70°C	24-PIN SILICONE DIP
2580I	0-70°C	24-PIN CERAMIC DIP

Note: "0" = 0V, "1" = +5V

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted. (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V, T_A = 25°C, V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		23	35	mA	(8)
I_{GG}	V_{GG} Power Supply Current		23	35	mA	(8)
V_{IL}	Input Logic "0"			+0.6	V	Note 12
V_{IH}	Input Logic "1"	+3.4		5.3	V	Note 12

AC CHARACTERISTICS

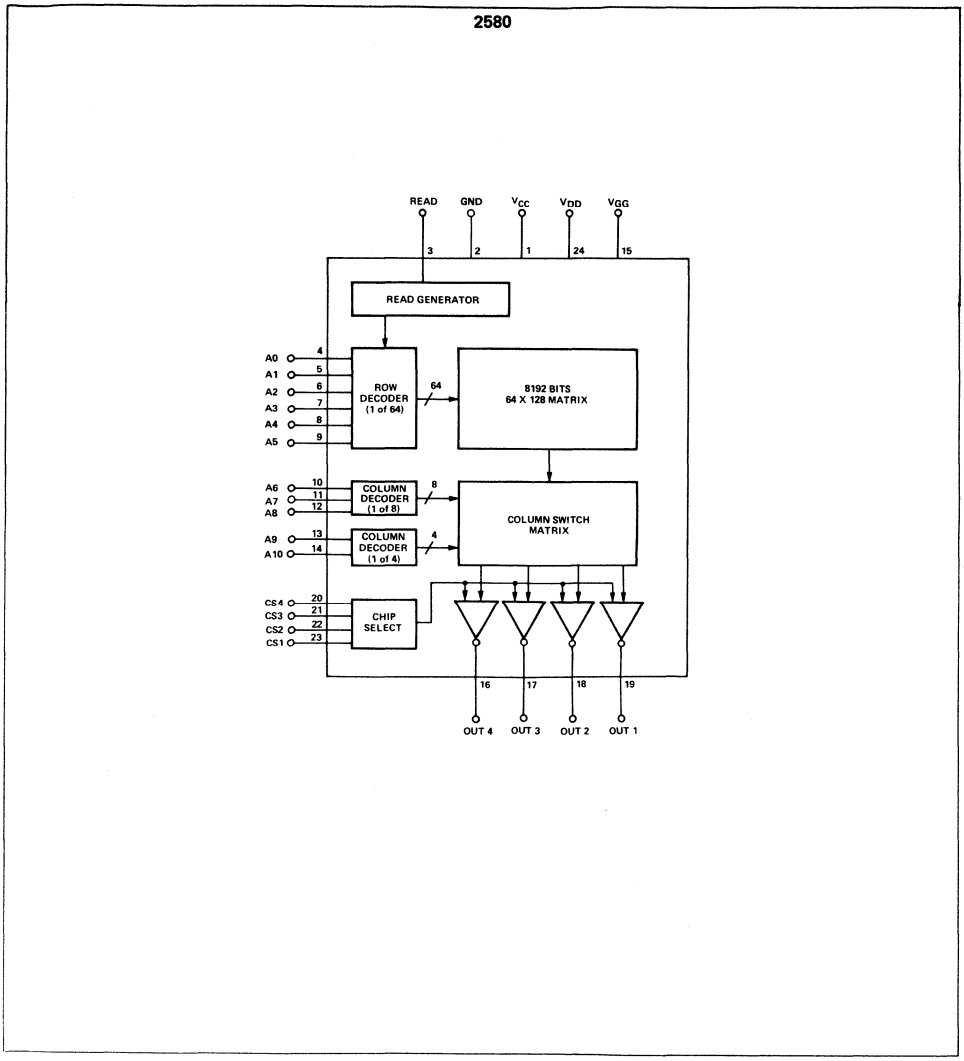
T_A = 25°C; V_{CC} = 5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0"			+0.5	V	I_{OI} = 1.6mA
V_{OH}	Output Logic "1"	+3.8			V	I_{OH} = 100μA
t_{RPW}[10]	Read Pulse Width	650	500		ns	
$t_{\overline{R}PW}$[9]	$\overline{\text{Read}}$ Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (11)			50	ns	
t_{AH}	Address Hold Time	0			ns	
t_{A1}	Address to Output Delay		625	950	ns	
t_{A2}	End of Read Pulse to Output Delay		250	350		
C_{IN}	Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs open, t_{RPW} = 500ns, $t_{\overline{R}PW}$ = 500ns.
9. During $t_{\overline{R}PW}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
10. During t_{RPW} addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (falling edge) of the READ pulse. After t_{A2}, data appears at the output terminals.
11. Addresses must be stable within 50ns after the READ line rises and must remain stable until the READ line falls.
12. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.

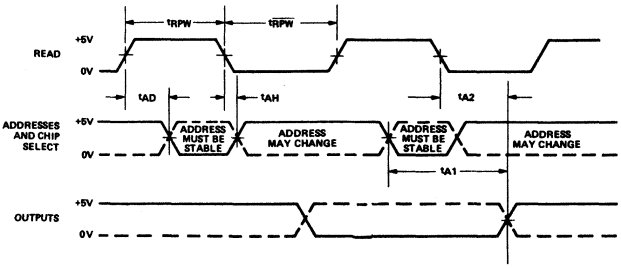
BLOCK DIAGRAM



(1)

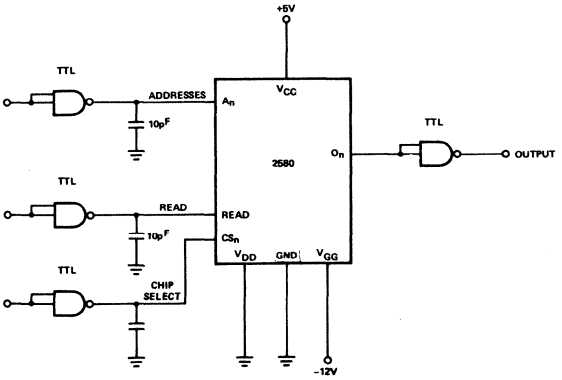
Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70° C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

TIMING DIAGRAM



Note: All measurements made at 50% points.
Input $t_r = t_f = 10ns$.

AC TEST SETUP

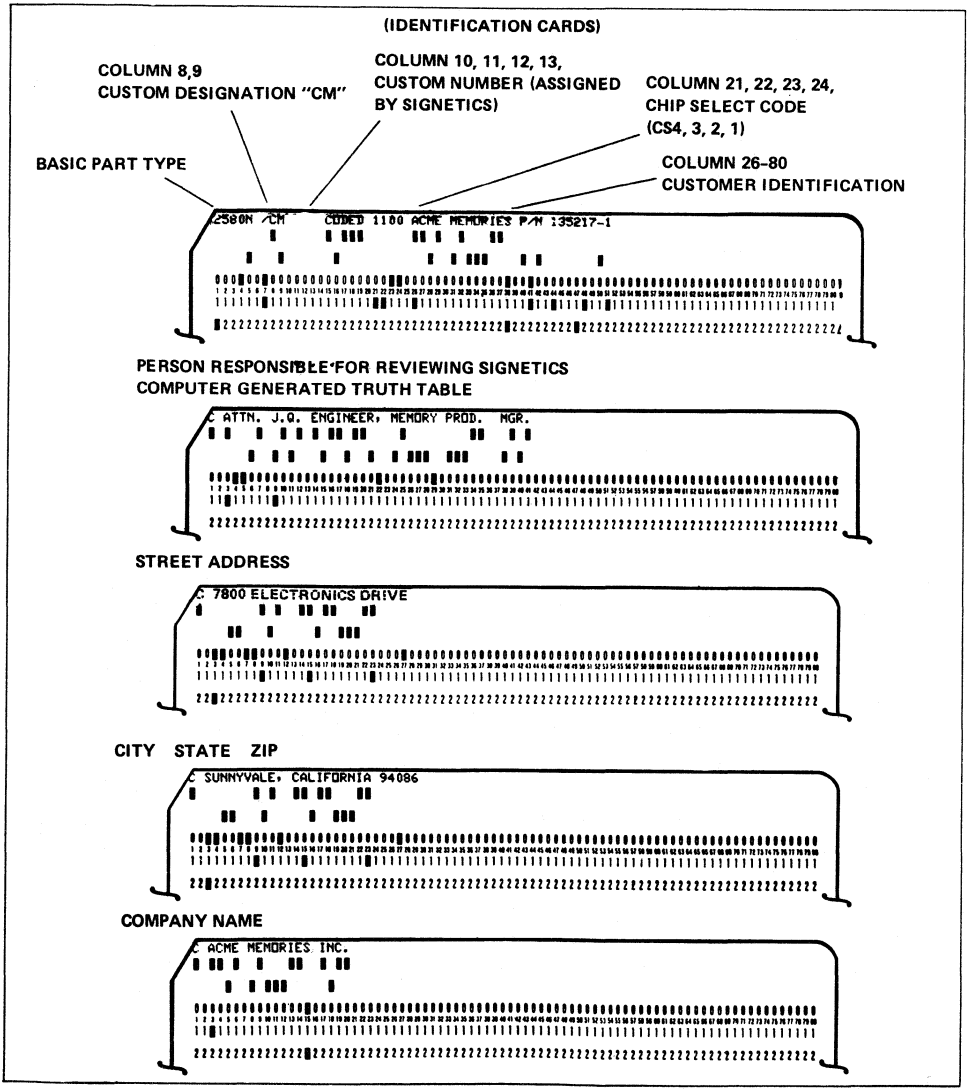


CODING FORMAT

Coding data for the 2580 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computor Aided Design (CAD) facility. The truth table will then be sent to the customer requesting engineer for final approval. On receipt of final approval, Signetics will cut the rubylith mask and proceed with manufacture.

CARD FORMAT



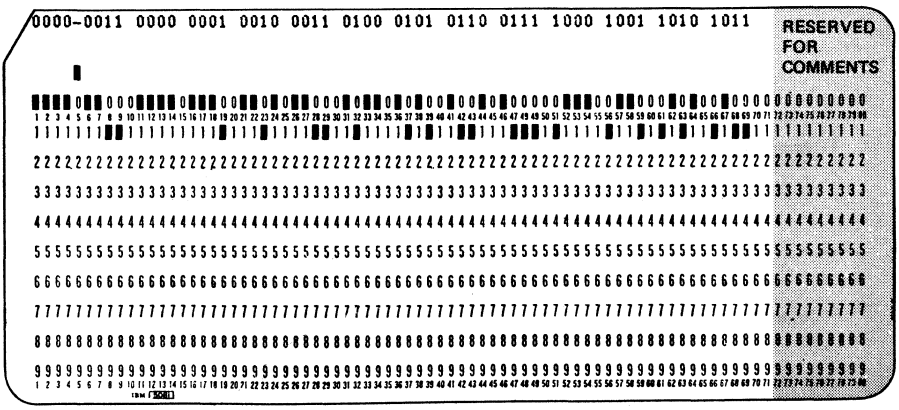
CODING FORMAT (Cont'd)

DATA CARD FORMAT

Col 1-4	Decimal equivalent of first data word location. Example: 0124 Note: leading zeros must be used for addresses from 0000 to 0999.
Col 5	Dash (-) to separate numbers
Col 6-9	Address of last data word on card
Col 10	Blank
Col 11-14	First data word ($0_4, 0_3, 0_2, 0_1$)
Col 15	Blank
Col 16-19	Second data word
Etc. thru column 71	
Col 72-80	Reserved for comments (These columns are ignored by the computer)

Up to twelve (12) data words can be coded on one card. Less than 12 may be used as long as the first and last addresses are given in columns 1-9.

EXAMPLE



signetics

1024X8 STATIC READ ONLY MEMORY | 2608

2608 I

N CHANNEL SILICON GATE MOS 2600 SERIES

DESCRIPTION

The 2608 is a fully decoded, static, mask programmable read-only memory. It has a capacity of 8192 bits organized 1024 X 8. The 2608 is fabricated with low threshold N-Channel silicon gate MOS technology which allows extreme ease of use with low voltage logic families such as transistor-transitor logic.

Requiring only 5 volts and ground power connections, the 2608 features a maximum access time of 650ns. Since the 2608 uses static logic throughout, no clocks are required. Four mask programmable chip selects are provided for easy word expansion. All 2608 inputs and outputs are TTL-compatible.

FEATURES

- 1024 X 8 ORGANIZATION
- STATIC OPERATION – NO CLOCKS
- 400ns ACCESS TIME
- SINGLE 5V POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS
- 400mW MAXIMUM POWER DISSIPATION
- TRI-STATE OUTPUTS
- 4 MASK PROGRAMMABLE CHIP SELECTS FOR EASY WORD EXPANSION
- N-CHANNEL SILICON GATE TECHNOLOGY
- STANDARD 24-PIN PACKAGE

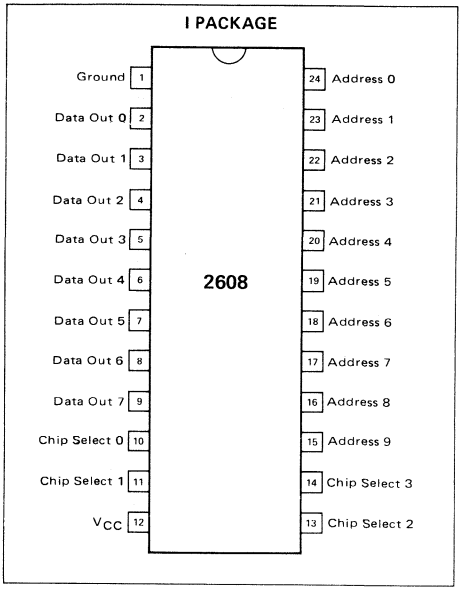
MAXIMUM GUARANTEED RATINGS[1]

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input, Output, and Supply Voltages with Respect to Ground Pin	-0.5V to +7V

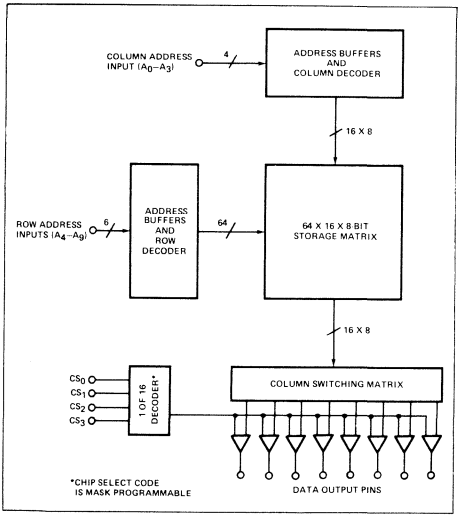
PART IDENTIFICATION

TYPE	OPERATING TEMPERATURE RANGE	PACKAGE
2608I	0°C – +70°C	24-pin ceramic dip

PIN CONFIGURATION



BLOCK DIAGRAM



DC OPERATING CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ (Unless Otherwise Noted)[3,4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{IN}	Input Load Current	$0 \leqslant V_{IN} \leqslant 5.25V$			10	μA
I_{LOH}	Output Leakage Current	$V_O = 2.4V$, Device Deselected			10	μA
I_{LOL}	Output Leakage Current	$V_O = 0.4V$, Device Deselected			10	μA
I_{CC}	Supply Current	$V_{CC} = 5.25V$, $T_A = 0°C$			80	mA
V_{IL}	Input Low Voltage		-0.5		0.65	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6mA$			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$	2.4			V
C_{IN}	Input Capacitance	$V_{IN} = 0V$			7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$			15	pF

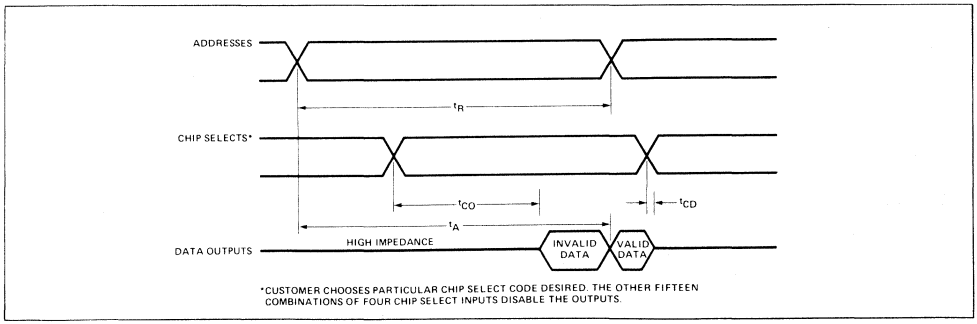
NOTES:
1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a $+150°C$ maximum junction temperature and a thermal resistance of $50°C/W$ junction to ambient.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process improvements.
7. Typical values are at $+25°C$, nominal supply voltages, and nominal processing parameters.

AC OPERATING CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ (See Notes A, B & C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_R	Read Cycle Time	650		ns	
t_{CO}	Chip Select to Output Enable		300	ns	Note D
t_{CD}	Chip Select to Output Disable	10	150	ns	Note D
t_A	Access Time	100	400	ns	Note D

NOTES:
A. Input levels swing between 0.65 volts and 2.2 volts.
B. Input signal transition times are 20 nsec.
C. Timing reference level is 1.5 volts.
D. Output load is one standard TTL load plus 130pF.

TIMING DIAGRAM



*CUSTOMER CHOOSES PARTICULAR CHIP SELECT CODE DESIRED. THE OTHER FIFTEEN COMBINATIONS OF FOUR CHIP SELECT INPUTS DISABLE THE OUTPUTS.

PIN DESCRIPTION

ADDRESSES

These ten TTL-compatible inputs are decoded on-chip to select one of 1024 eight-bit bytes. Since the 2608 utilizes static logic throughout, a change in addresses results in a change in data as long as the chip is selected. Access time is measured from the point where the last address input became stable. Cycle time and access time are equal in a static ROM design.

CHIP SELECTS

There are four TTL-compatible chip select inputs for the 2608. Only one combination of these four signals enables the chip. The other fifteen disable the chip. The particular enabling combination is chosen by the customer and specified on the first punched card of the customer card deck (see following page). A positive logic convention is assumed.

DATA OUTPUTS

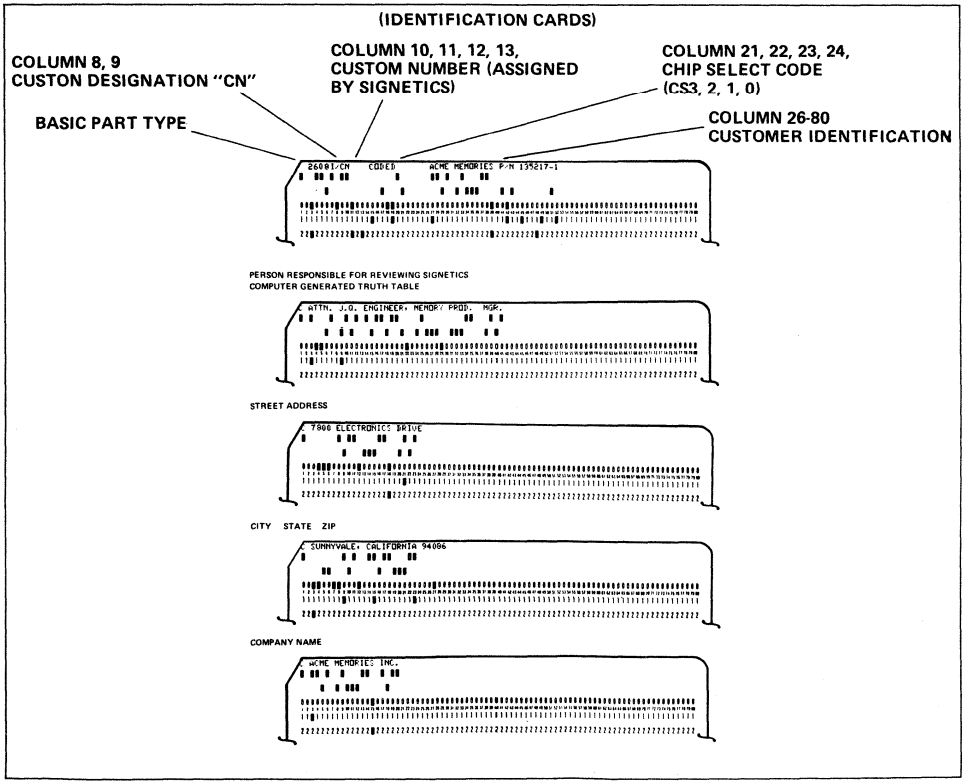
The eight data outputs are push-pull buffers capable of driving one standard TTL-load plus a 130pF load capacitance. These outputs are placed in the high impedance state when any one of the disabling combinations of the chip select inputs is present.

CODING FORMAT

Coding data for the 2608 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

CARD FORMAT



DATA CARDS

Columns

12——75	Hexadecimal data coding
77——78	Card number (starting 01)
79——80	Total number of cards (32)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 32 cards will contain 1024 bytes of 8 bits.

BINARY TO HEXADECIMAL CONVERSION

BINARY COMBINATION D0-D3 OR D4-D7				HEXADECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F